TECHNICAL MANUAL

ORGANIZATIONAL MAINTENANCE MANUAL
DISPLAY EQUIPMENT MAINTENANCE

EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)

GUIDED MISSILE AIR DEFENSE SYSTEM
AN/TSQ-73

HEADQUARTERS, DEPARTMENT OF THE ARMY
10 JANUARY 1985

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EXPANDED TROUBLESHOOTING
(LOGIC DIAGRAMS)
GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73.**

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WARNING

DANGEROUS VOLTAGE

is used in the operation of this equipment

DEATH ON CONTACT

may result if personnel fail to observe safety precautions

Never work on electronic equipment unless there is another person nearby who is familiar with the operation and hazards of the equipment and who is competent in administering first aid. When the technician is aided by operators, he must warn them about dangerous areas.

Whenever possible, the power supply to the equipment must be shut off before beginning work on the equipment. Take particular care to ground every capacitor likely to hold a dangerous potential. When working inside the equipment, after the power has been turned off, always ground every part before touching it.

Be careful not to contact high-voltage connections when installing or operating this equipment.

Whenever the nature of the operation permits, keep one hand away from the equipment to reduce the hazard of current flowing through vital organs of the body.

WARNING

Do not be misled by the term "low voltage." Potentials as low as 50 volts may cause death under adverse conditions.

EXTREMELY DANGEROUS POTENTIALS

greater than 500 volts exist in the following units:

Display console high voltage power supply

Display console CRT

WARNING

For emergencies requiring immediate shutdown of system power, press SYSTEM POWER OFF switch located on power cabinet power transfer unit. Observe that SYSTEM POWER ON indicator light goes off.

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ORGANIZATIONAL MAINTENANCE MANUAL: DISPLAY EQUIPMENT MAINTENANCE

EXPANDED TROUBLESHOOTING (LOGIC DIAGRAMS) .

GUIDED MISSILE AIR DEFENSE SYSTEM AN/TSQ-73

REPORTING ERRORS AND RECOMMENDING IMPROVEMENTS

You can help improve this manual. If you find any mistakes, or if you know of a way to improve the procedures, please let us know. Mail your letter, DA Form 2028 (Recommended Changes to Publications and Blank Forms) or DA Form 2028-2, located in back of this manual, direct to: Commander, U.S. Army Missile Command, ATTN: AMSMI-LC-ME-P, Redstone Arsenal, AL 35898-5238. A reply will be furnished to you.

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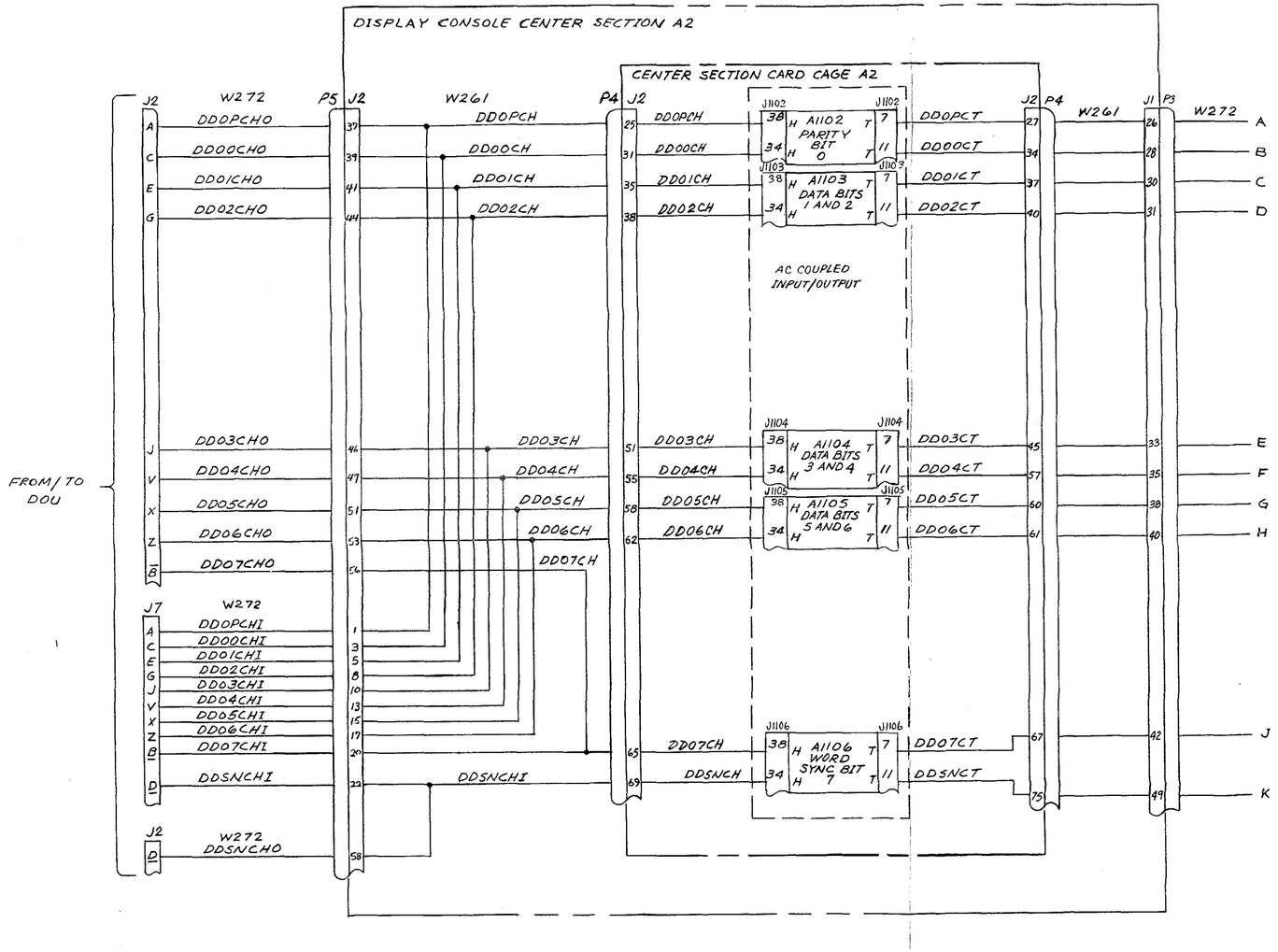
INPUTS	F/O - SH	OUTPUTS	F/O - SH
A10MA04	54-2	ADDDT0	4-1
ABLTC2E	4-1	ADDFBR	4-1
ADDBL0	4-1	ADDFB6	4-1
AIBR5D4	53-0	ADDL0R	2-0
LADR50	53-0	ADDL1R	2-0
LIBENA	51-0	ADDL2R	2-0
LIBPFJ	49-0	ADDL3R	2-0
LMMAN8	49-0	ADDL4R	2-0
LTSAG2E	48-1	ADDL5R	2-0
LTSCG0E	48-1	ADDL6R	2-0
LTSCG1E	48-1	ADDL7R	2-0
LTSCG2E	48-1	ADMFTA	2-0
LTSCG3E	48-1		
LTSDG0E	48-1		
LTSDG1E	48-1		
LTSDG2E	48-1		
LTSDG3E	48-1		



FO-1. Alterable Processor High Speed Input Buffer Input Logic Diagram (Sheet 1 of 2)

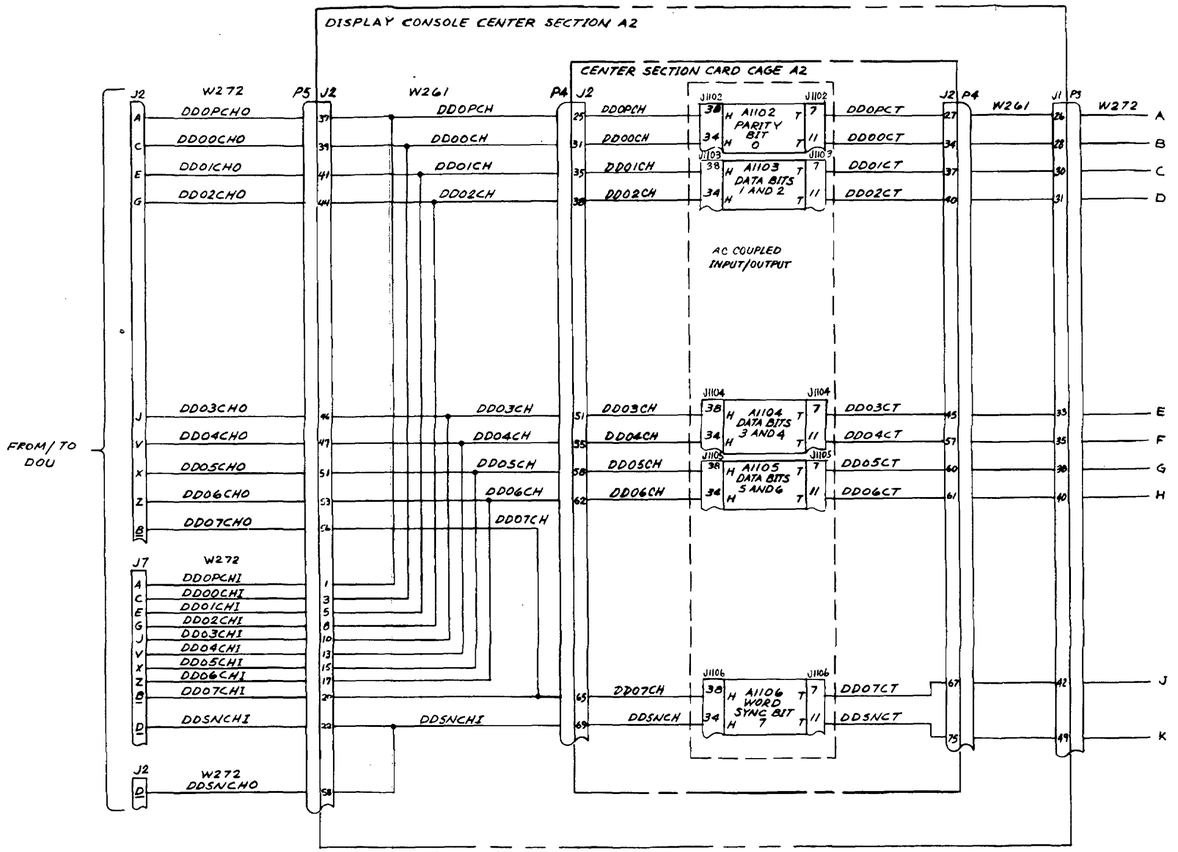
NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

INPUTS	F/O - SH	OUTPUTS	F/O - SH
A10MA04	54-2	ADDDT0	4-1
ABLTC2E	4-1	ADDFBR	4-1
ADDBL0	4-1	ADDFBS	4-1
AIBRSD4	53-0	ADDL0R	2-0
LADR80	53-0	ADDL1R	2-0
LIBENA	51-0	ADDL2R	2-0
LIBPFJ	49-0	ADDL3R	2-0
LMMANS	49-0	ADDL4R	2-0
LTSAG2E	48-1	ADDL5R	2-0
LTSCG0E	48-1	ADDL6R	2-0
LTSCG1E	48-1	ADDL7R	2-0
LTSCG2E	48-1	ADMFTA	2-0
LTSCG3E	48-1		
LTSDG0E	48-1		
LTSDG1E	48-1		
LTSDG2E	48-1		
LTSDG3E	48-1		



NOTES: UNLESS OTHERWISE SPECIFIED

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2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

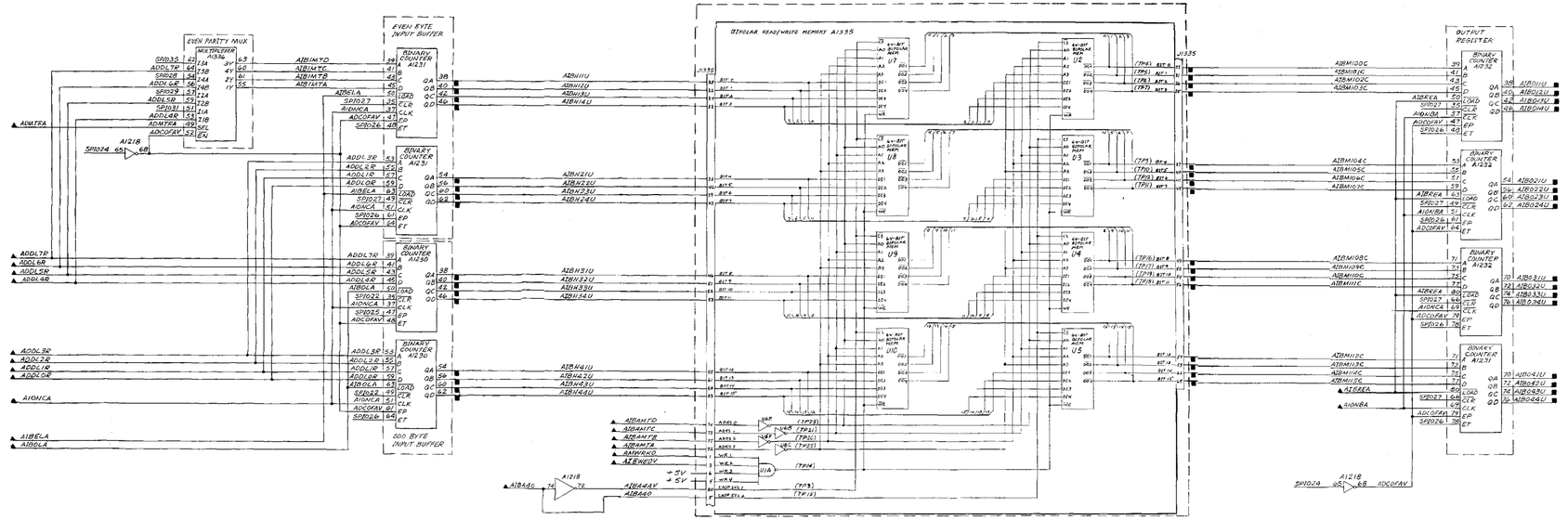
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

MS200113A

Change 1 FO-1. Alterable Processor High Speed Input Buffer Input Logic Diagram (Sheet 1 of 2)

INPUTS	I/O - BN	OUTPUTS	I/O - BM
ADDL6R	1-2	AIBM111U	52-2
ADDL1R	1-2	AIBH112U	52-2
ADDL2R	1-2	AIBH133U	53-3
ADDA3R	1-2	AIBH134U	53-2
ADDL4R	1-3	AIBM21U	53-3
ADDL5R	1-2	AIBH22U	52-2
ADDL1R	1-3	AIBM24U	51-3
AIMTFA	1-2	AIBH23U	52-2
AIBAMTA	3-0	AIBH33U	52-2
AIBAMTB	3-0	AIBH34U	52-2
AIBAMTC	3-0	AIBM41U	52-2
AIBAMTD	3-0	AIBH42U	52-2
AIBA40	3-0	AIBH43U	53-2
AIBELA	4-1	AIBM44U	53-3
AIBJEA	4-2	AIBM100C	52-3
AIBWE0V	4-2	AIBM103C	53-3
AIBOLA	4-1	AIBM102C	52-3
AMWRKO	54-2	AIBM108C	52-3
A100BA	54-2	AIBM105C	53-3
A100CA	54-2	AIBM104C	53-3
		AIBM106C	53-3
		AIBM107C	52-3
		AIBM109C	53-3
		AIBM110C	52-3

OUTPUTS	I/O - BM	OUTPUTS	I/O - BS
AIBM109C	52-2	AIB021U	8-1
AIBM112C	52-2	AIB023U	8-1
AIBM113C	53-2	AIB024U	8-1
AIBM112C	52-2	AIB031U	8-2
AIBM113C	52-2	AIB032U	8-2
AIBM114C	52-2	AIB033U	8-2
AIBM113C	52-2	AIB034U	8-2
AIB0113U	8-1	AIB041U	8-3
AIB0123U	8-1	AIB042U	8-2
AIB0133U	8-1	AIB043U	8-2
AIB0134U	8-1	AIB044U	8-2
AIB0131U	8-1		



FO-2. Alterable Processor High Speed Input Buffer Read/Write Memory and Output Register Logic Diagram

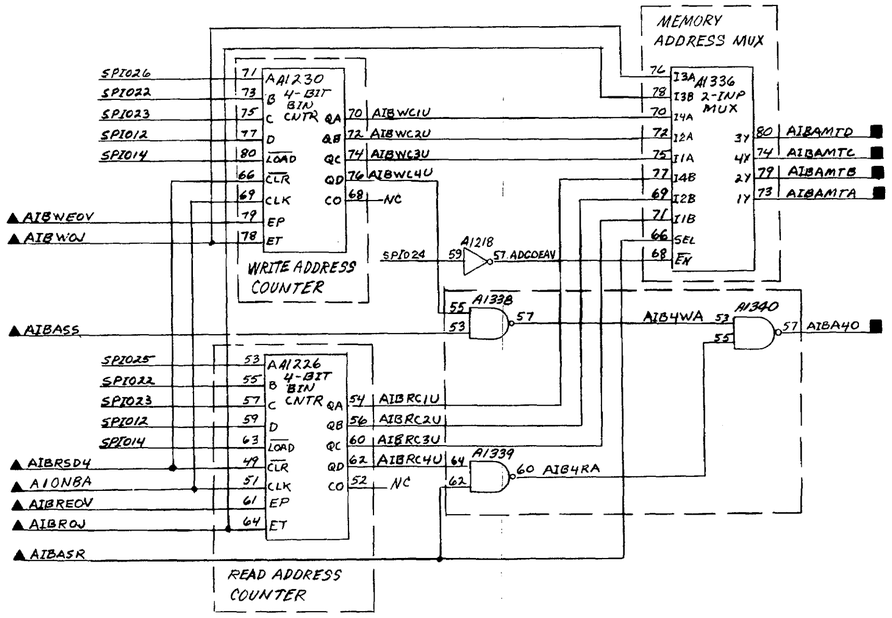
NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS, PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE AR CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOL ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGUR
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURI
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCU CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

INPUTS	F/O - SH	OUTPUTS	F/O - SH
AIBASS	4-2	AIBA40	2-0
AIBASR	4-2	AIBAMTA	2-0
AIBRE0V	4-2	AIBAMTB	2-0
AIBR0J	4-2	AIBAMTC	2-0
AIBRSD4	53-0	AIBAMTD	2-0
AIBWE0V	4-2		
AIBW0J	4-2		
A10NBA	54-2		



FO-3. Alterable Processor High Speed Input Buffer Read/Write Address Counter Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

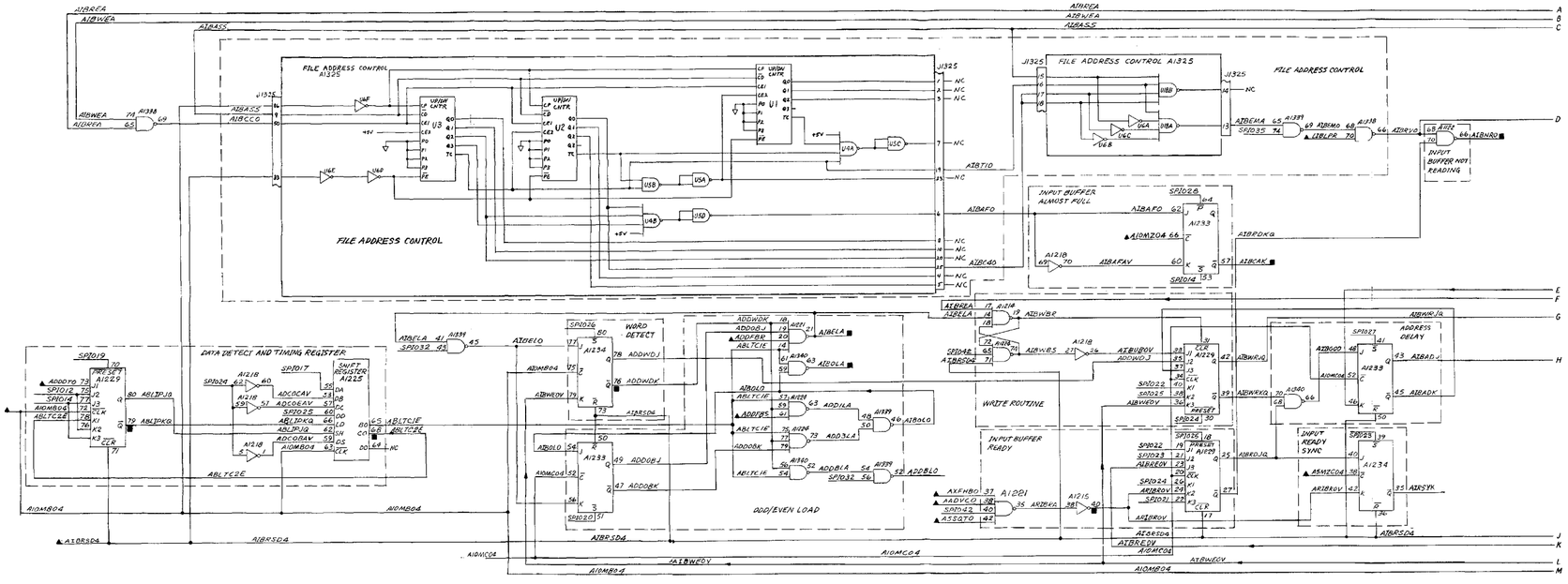
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

MS200115

INPUTS	F/O - SH	OUTPUTS	F/O - SH
A1MZC04	14-2	ABUIPKQ	52-1
A1SQT6	14-2	ABUTCIE	1-2
A1OMB04	14-2	ADDBL8	1-2
A1OMC04	14-2	ADDWDK	52-1
A1OMZ04	14-2	A2BASK	3-0
AADVC0	12-0	A2BASS	3-0
ADODT0	1-2	A2BCAK	14-2
ADOFBR	1-2	A2BELA	2-0
ADOFBS	1-2	A2BWR0	52-1
A2BRD4	53-0	A2BWLA	2-0
AXFH80	14-1	A2BWEA	2-0
L1SLPR	63-0	A2BWE0V	3-0
		A2BWE1V	3-0
		A2BWE2V	2-0
			2-0
		A2BWQJ	3-0
		A2RSYK	14-3
		A2ZR0V	13-0



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER ANI ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
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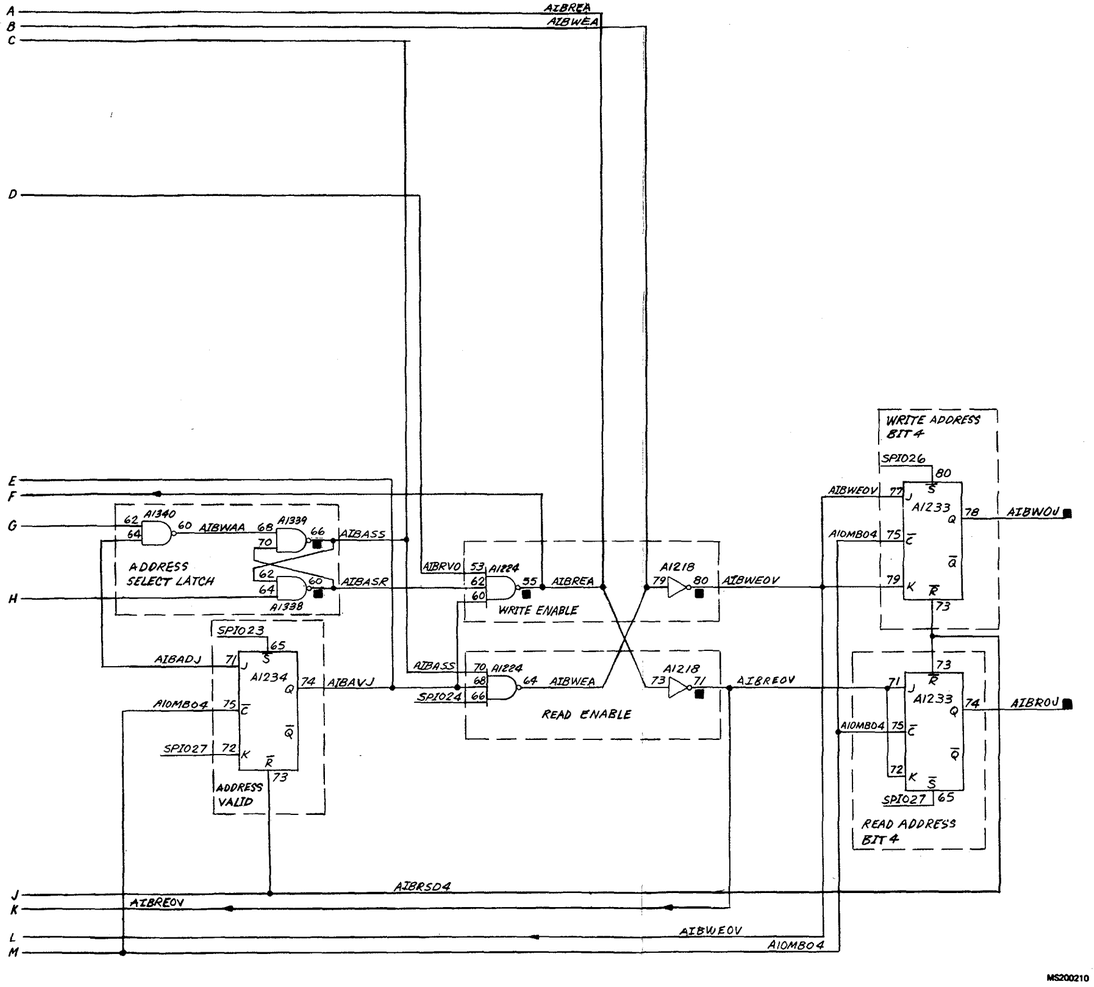
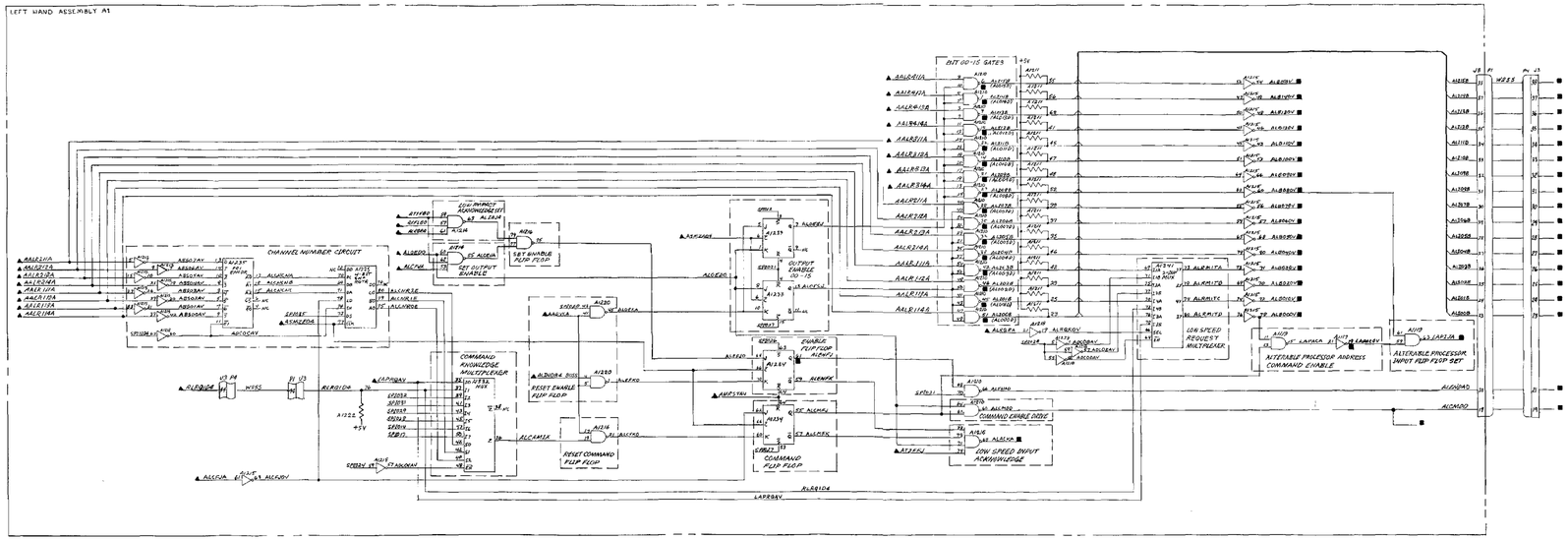
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AI GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATION AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THR 5-8 FOR COMMON LISTING.

MS200116

FO-4. Alterable Processor High Speed Input Buffer Control Logic Diagram (Sheet 1 of 2)



FO-4. Alterable Processor High Speed Input Buffer Control Logic Diagram (Sheet 2 of 2)


LEFT WAND ASSEMBLY A1
CHANNEL NUMBER CIRCUIT
COMMAND KNOWLEDGE MULTIPLEXER
BIT 00-15 GATES
LOW SPEED REQUEST MULTPLEXER
ALTERABLE PROCESSOR ADDRESS COMMAND ENABLE
ALTERABLE PROCESSOR INPUT FLIP FLOP SET
COMMAND CABLE DRIVE
LOW SPEED INPUT ACKNOWLEDGE
SET ENABLE FLIP FLOP
RESET ENABLE FLIP FLOP
SET COMMAND FLIP FLOP
RESET COMMAND FLIP FLOP
OUTPUT ENABLE (0-15)
ENABLE FLIP FLOP
LOW IMPACT ACKNOWLEDGE (1)
SET OUTPUT ENABLE
DC ALCLR
DC ALCLK
DC ALCLR2
DC ALCLK2
ALCLR1A
ALCLK1A
ALCLR2A
ALCLK2A
ALCMD1A
ALCMD2A
ALCMD3A
ALCMD4A
ALCMD5A
ALCMD6A
ALCMD7A
ALCMD8A
ALCMD9A
ALCMD10A
ALCMD11A
ALCMD12A
ALCMD13A
ALCMD14A
ALCMD15A
ALCMD16A
ALCMD1
ALCMD2
ALCMD3
ALCMD4
ALCMD5
ALCMD6
ALCMD7
ALCMD8
ALCMD9
ALCMD10
ALCMD11
ALCMD12
ALCMD13
ALCMD14
ALCMD15
ALCMD16
ALCMD
ALCMDO
ALCMDO2
ALCMDO3
ALCMDO4
ALCMDO5
ALCMDO6
ALCMDO7
ALCMDO8
ALCMDO9
ALCMDO10
ALCMDO11
ALCMDO12
ALCMDO13
ALCMDO14
ALCMDO15
ALCMDO16
ALCMDO17
ALCMDO18
ALCMDO19
ALCMDO20
ALCMDO21
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ALCMDO26
ALCMDO27
ALCMDO28
ALCMDO29
ALCMDO30
ALCMDO31
ALCMDO32
ALCMDO33
ALCMDO34
ALCMDO35
ALCMDO36
ALCMDO37
ALCMDO38
ALCMDO39
ALCMDO40
ALCMDO41

INPUTS	F/O - 8E
AALR100	14-1
AALR111A	8-1
AALR112A	8-1
AALR113A	8-1
AALR114A	8-1
AALR115A	18-0
AALR120A	18-0
AALR130A	18-0
AALR134A	18-0
AALR211A	8-1
AALR212A	8-1
AALR213A	6-1
AALR214A	8-1
AALR230A	18-0
AALR233A	18-0
AALR234A	18-0
AALR311A	8-2
AALR312A	8-2
AALR313A	8-2
AALR314A	8-2
AALR331A	18-0

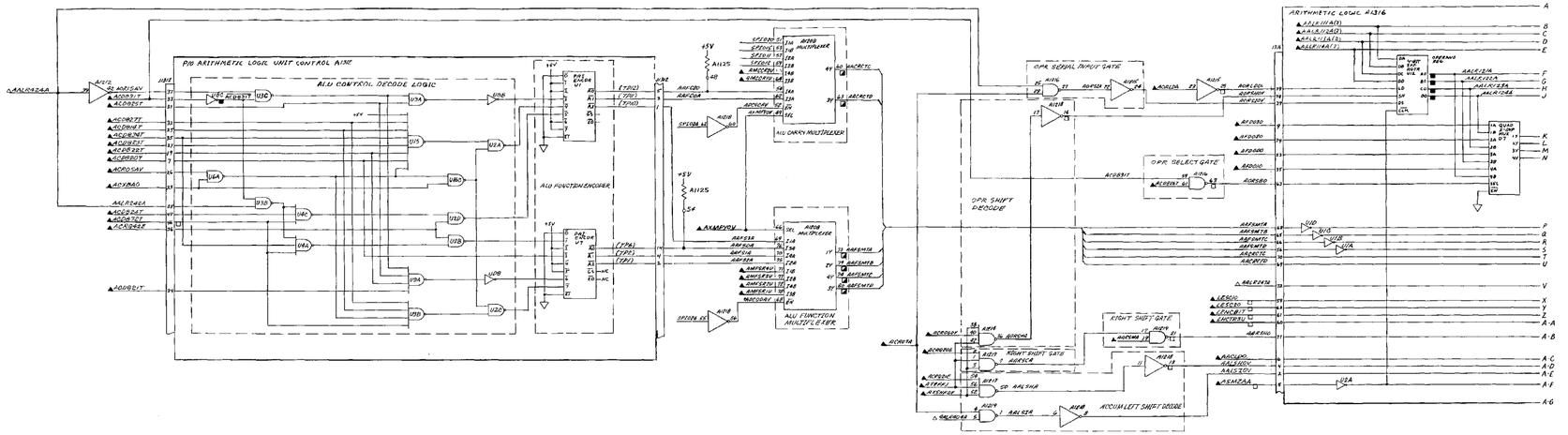
INPUTS	F/O - 9H
AFD120	7-2
AFD140	7-2
AFD150	7-2
AMCCR1U	12-0
AMCCR2U	12-0
AMFR1U	12-0
AMFR2U	12-0
AMFR3U	12-0
AMF04U	12-0
AOR12A	14-0
ATFF2	12-0
AXCBA0	11-0
AXMF05V	14-0
AXSH5V	14-0
LENCBT	12-1
LESC10	12-1
LESC20	12-1
LESC40	12-1
LMCTR3C	12-1
LMCT3AV	12-1

INPUTS	F/O - 9E
AALR2032A	10-0
AALR2035A	10-0
AALR2034A	10-0
AALR4111A	8-2
AALR4112A	8-2
AALR4113A	8-2
AALR4114A	10-0
AALR4131A	10-0
AALR4132A	10-0
AALR4133A	10-0
AALR4134A	10-0
AAR03A	12-0
ASM7AA	14-2
ACD01BT	14-0
ACD02BT	14-0
ACD03BT	14-0
ACD04BT	14-0
ACD05BT	14-0
ACD06BT	14-0
ACD07BT	14-0
AFD030	7-2
AFD060	7-2
AFD090	7-2
AFD100	7-2
AFD110	7-2
AFD120	7-2

OUTPUTS	F/O - 8E
AACBOTC	12-2
AACBOTD	12-2
AAFSMTA	12-2
AAFSMTB	12-2
AAFSMTC	12-2
AAFSMTD	12-2
AALR1031A	8-1
AALR1032A	8-1
AALR1033A	8-1
AALR1034A	8-1
AALR1121A	9-1
AALR122A	8-1
AALR123A	8-1
AALR124A	8-1
AALR201A	8-1
AALR202A	8-1
AALR203A	8-1
AALR204A	8-1
AALR221A	8-1
AALR222A	8-1
AALR223A	8-1
AALR224A	8-1
AALR261A	8-2
AALR3HA	8-3

OUTPUTS	F/O - 8H
ACD01T	14-1
ACD02T	14-1
ACD03T	14-1
ACD04T	14-1
ACD05T	14-1
ACD06T	14-1
ACD07T	14-1
AFD030	7-2
AFD060	7-2
AFD090	7-2
AFD100	7-2
AFD110	7-2
AFD120	7-2

OUTPUTS	F/O - 8G
AALR3031A	8-2
AALR3034A	8-2
AALR3111A	8-2
AALR3221A	8-2
AALR3223A	8-2
AALR3261A	8-2
AALR3401A	8-2
AALR3402A	8-2
AALR3403A	8-2
AALR3404A	8-2
AALR3421A	8-2
AALR3422A	8-2
AALR3423A	8-2
AALR3424A	8-2
AAL15A	14-2
AATSCIA	14-2
ABM01B	12-2
ABM03B	12-2
ACD01T	14-2
ACR07W	8-1
APB01S	10-2
APB04M	10-2
ARKDFA	9-1
ASMEAA	10-0



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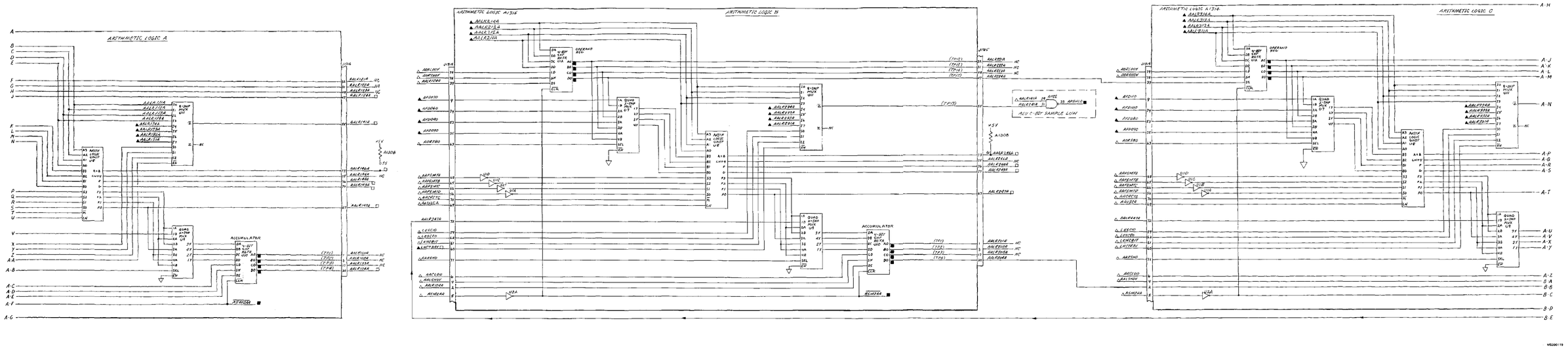
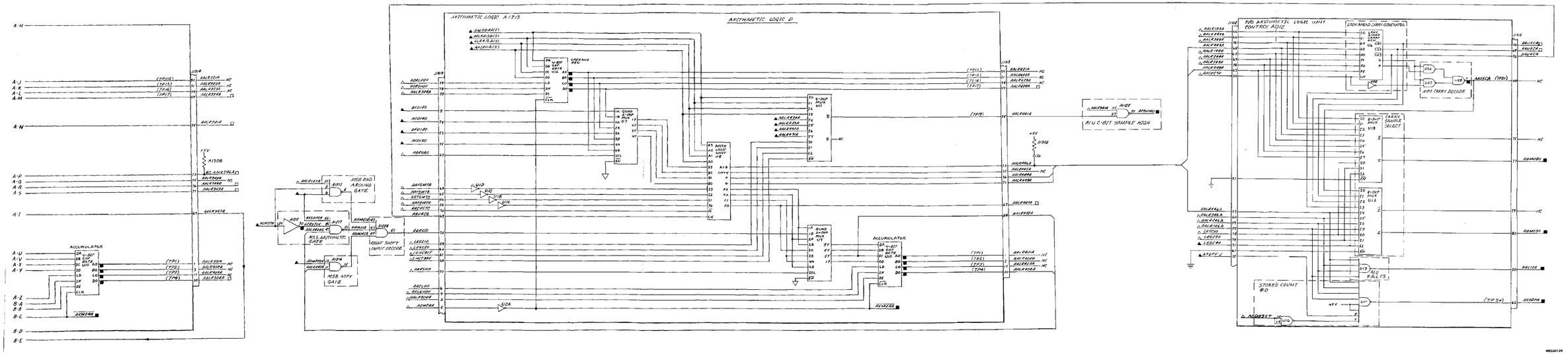
MB300118

FO-6. Alterable Processor Arithmetic Logic Diagram (Sheet 1 of 3)



FO-6. Alterable Processor Arithmetic Logic Diagram (Sheet 2 of 3)


ARITHMETIC LOGIC A13I3
ARITHMETIC LOGIC D
ACCUMULATOR
ACCUMULATOR
MSB END AROUND GATE
MSB MPY GATE
RIGHT SHIFT / INPUT DECODE
A13C8
A13R8
A13R9
A13R10
A13R11
A13R12
A13R13
A13R14
A13R15
A13R16
A13R17
A13R18
A13R19
A13R20
A13R21
A13R22
A13R23
A13R24
A13R25
A13R26
A13R27
A13R28
A13R29
A13R30
A13R31
A13R32
A13R33
A13R34
A13R35
A13R36
A13R37
A13R38
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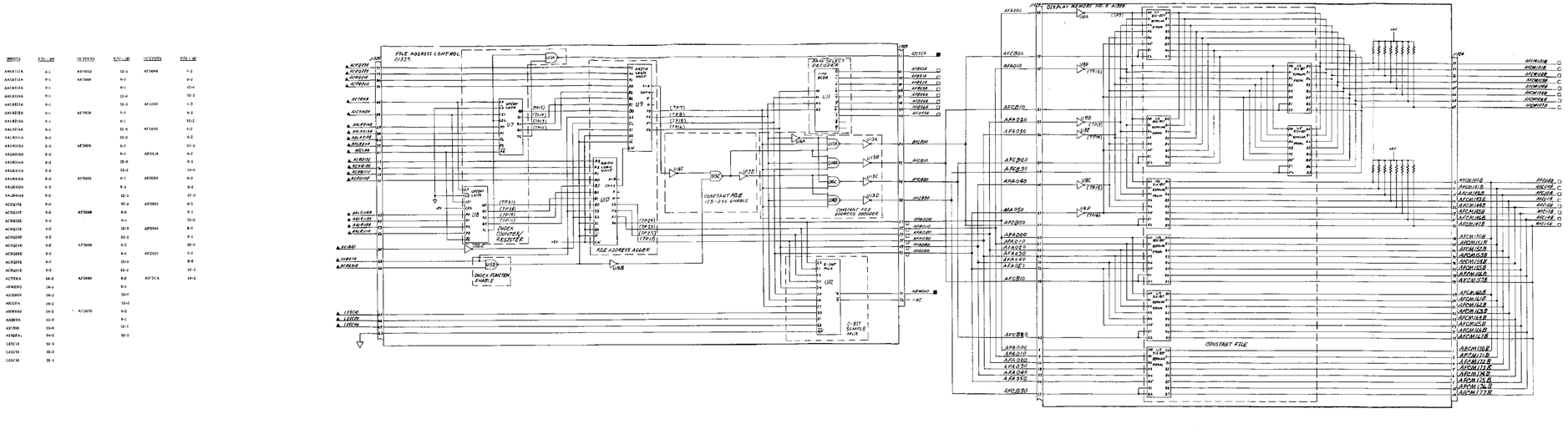
A13R41
A13R42
A13R43
A13R44
A13R45
A13R46
A13R47



NOTES: UNLESS OTHERWISE SPECIFIED

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2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
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   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

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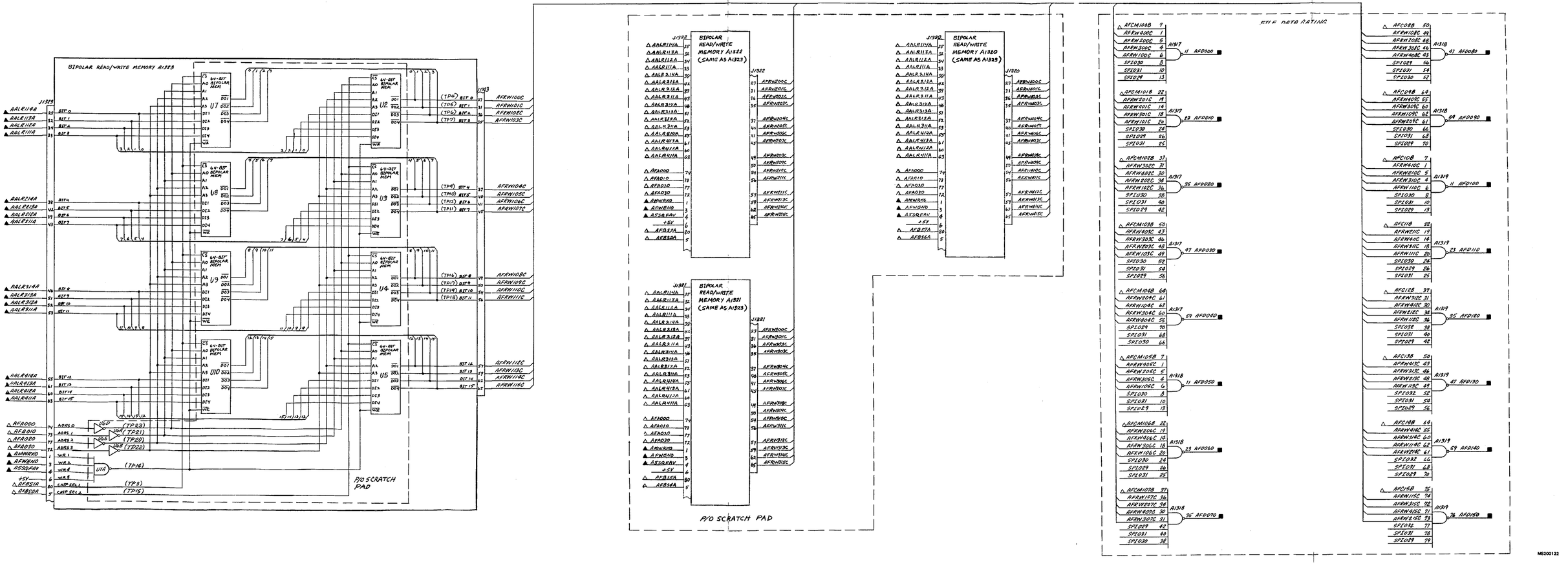
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

FO-7. Alterable Processor Data File Storage and Address Logic Diagram (Sheet 1 of 2)



FO-7. Alterable Processor Data File Storage and Address Logic Diagram (Sheet 2 of 2)

INPUTS	F/O - SH
AALR101A	5-2
AALR102A	6-2
AALR103A	6-2
AALR104A	6-2
AALR121A	8-1
AALR122A	8-1
AALR123A	8-1
AALR124A	8-1
AALR201A	8-2
AALR202A	8-2
AALR203A	8-2
AALR204A	8-2
AALR221A	8-2
AALR222A	8-2
AALR223A	8-2
AALR224A	8-2
AALR301A	6-3
AALR302A	6-3
AALR303A	6-3
AALR304A	6-3
AALR321A	6-2
AALR322A	6-2

INPUTS	F/O - SH
APAC11U	9-1
APAC12U	9-1
APAC13U	9-1
APAC14U	9-1
APAC31U	9-1
APAC32U	9-1
APAC23U	9-1
APAC24U	9-1
APAC33U	9-1
APAC34U	9-1
KSW06D4	28-2
KSW07D4	28-2
KSW08D4	28-2
LD0RN0V	50-2
LDRQ0AV	50-2
LMFC0W	50-2
LMFE0W	50-2
LMT06A0V	50-2
LRODEJ	53-C
LRQ0V01	50-2

INPUTS	F/O - SH
ACRQ11E	9-2
ACRQ12E	9-2
ACRQ13E	9-2
ACRQ20E	9-2
ACRQ22E	9-2
ACRQ23E	9-2
ACRQ31E	9-2
ACRQ32E	9-2
ACRQ33E	9-2
AFD000	9-2
AFD010	9-2
AFD020	9-2
AFD030	9-2
AFD040	9-2
AFD050	9-2
AFD060	9-2
AFD070	9-2
AFD080	9-2
AFD090	9-2
AFD100	9-2
AFD110	9-2

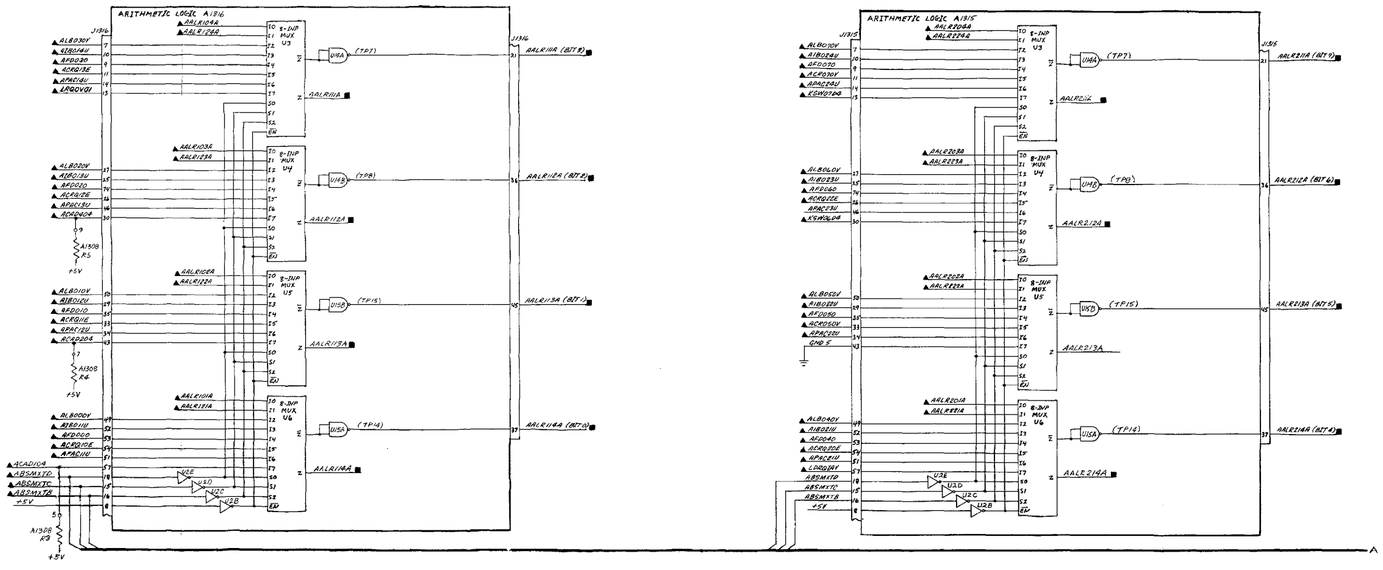
OUTPUTS	F/O - SH
AALR111A	5-0
	6-1
	7-1
	7-2
	9-1
	10-0
AALR112A	5-0
	6-2
	7-1
	7-2
	9-1
	10-0
AALR113A	5-0
	6-2
	7-1
	7-2
	9-1
	10-0
AALR114A	5-0
	6-2
	7-1
	7-2
	9-1
	10-0

INPUTS	F/O - SH
AFD120	9-2
AFD130	9-2
AFD140	9-2
AFD150	9-2
AFD160	9-2
AFD170	9-2
AFD180	9-2
AID031U	2-0
AID032U	2-0
AID033U	2-0
AID034U	2-0
AID035U	2-0
AID036U	2-0
AID037U	2-0
AID038U	2-0
AID039U	2-0
AID040U	2-0
AID041U	2-0
AID042U	2-0
AID043U	2-0
AID044U	2-0
ALR009V	5-6
ALR010V	5-6

OUTPUTS	F/O - SH
AALR211A	5-0
	6-2
	7-1
	7-2
	9-1
	10-0
AALR212A	5-0
	6-2
	7-2
	9-1
	10-0
AALR213A	5-0
	6-2
	7-1
	7-2
	9-1
	10-0
AALR214A	5-0
	6-2
	7-1
	7-2
	9-1
	10-0
AALR413A	5-0
	6-2
	7-2
	9-1
	10-0

INPUTS	F/O - SH
ALR203V	5-0
ALR204V	5-0
ALR205V	5-0
ALR206V	5-0
ALR207V	5-0
ALR208V	5-0
ALR209V	5-0
ALR210V	5-0
ALR211V	5-0
ALR212V	5-0
ALR213V	5-0
ALR214V	5-0
ALR215V	5-0

OUTPUTS	F/O - SH
AALR412A	5-0
	6-2
	7-2
	10-0
AALR413A	5-0
	6-2
	7-2
	10-0
AALR414A	5-0
	6-2
	7-2
	10-0



NOTES: UNLESS OTHERWISE SPECIFIED

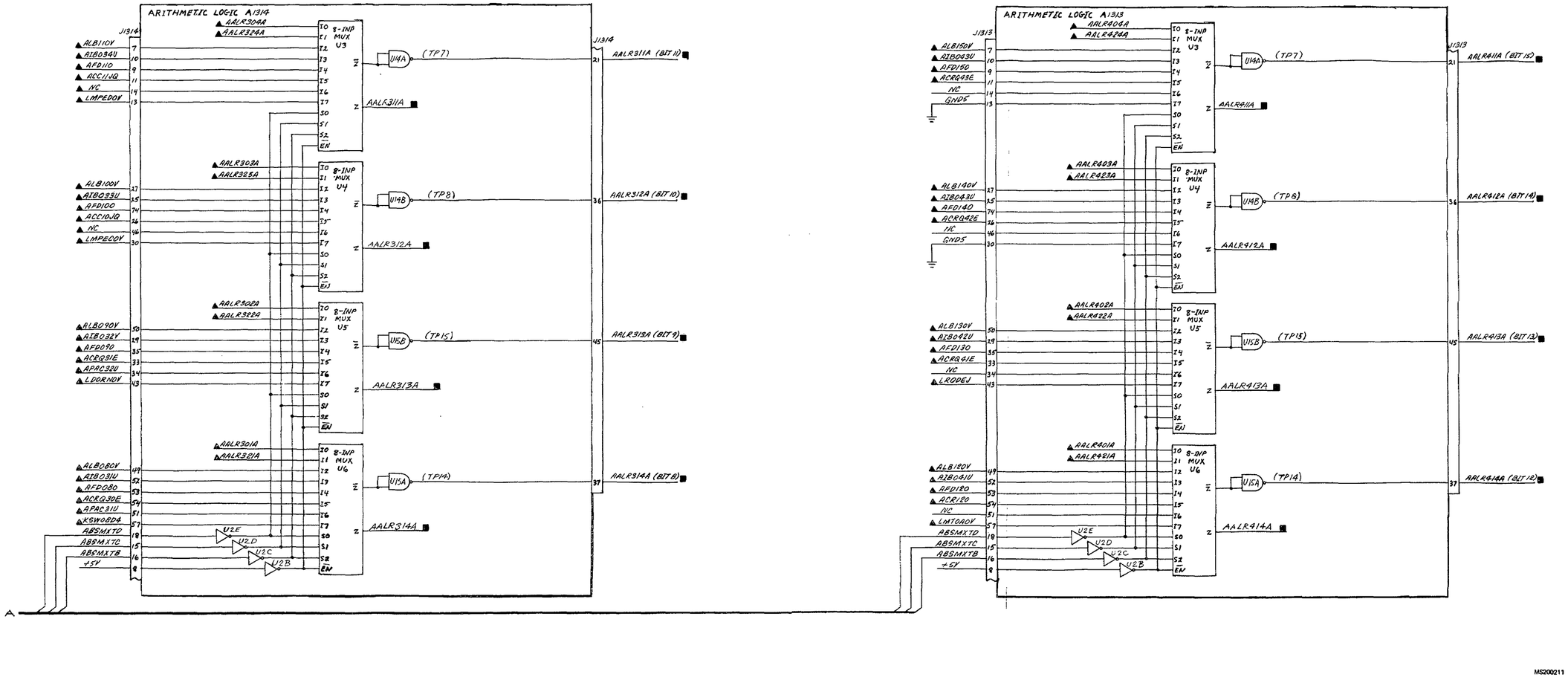
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

MS200123

FO-8. Alterable Processor 8-Input Multiplexer Logic Diagram (Sheet 1 of 2)



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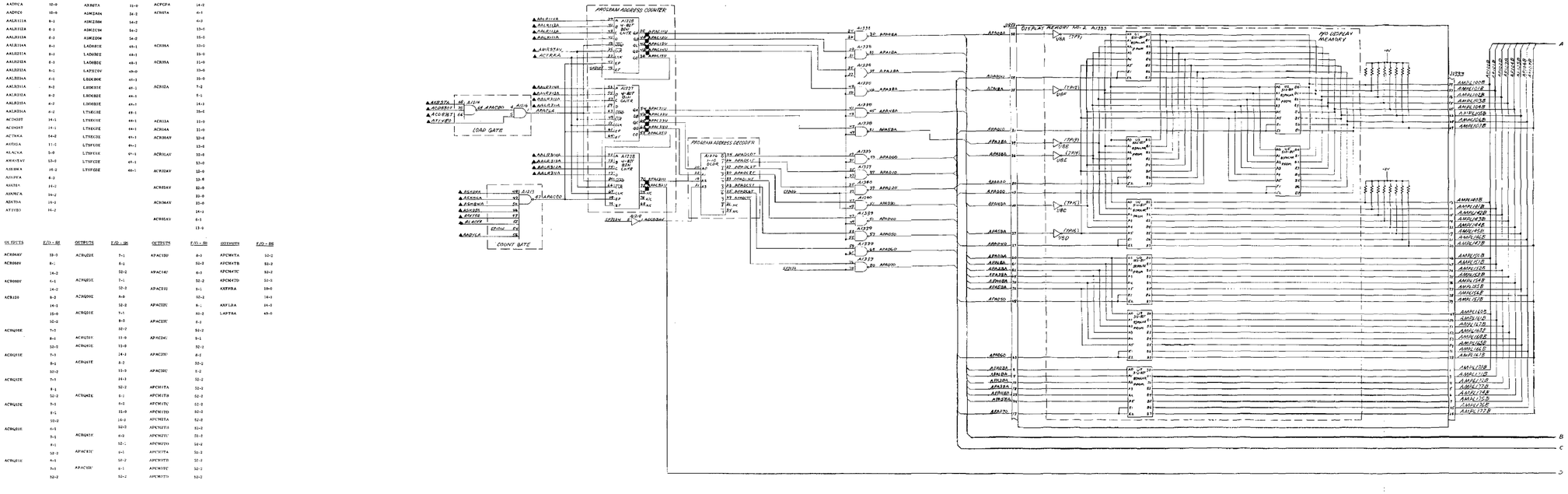
FO-8. Alterable Processor 8-Input Multiplexer Logic Diagram (Sheet 2 of 2)



NOTES: UNLESS OTHERWISE SPECIFIED

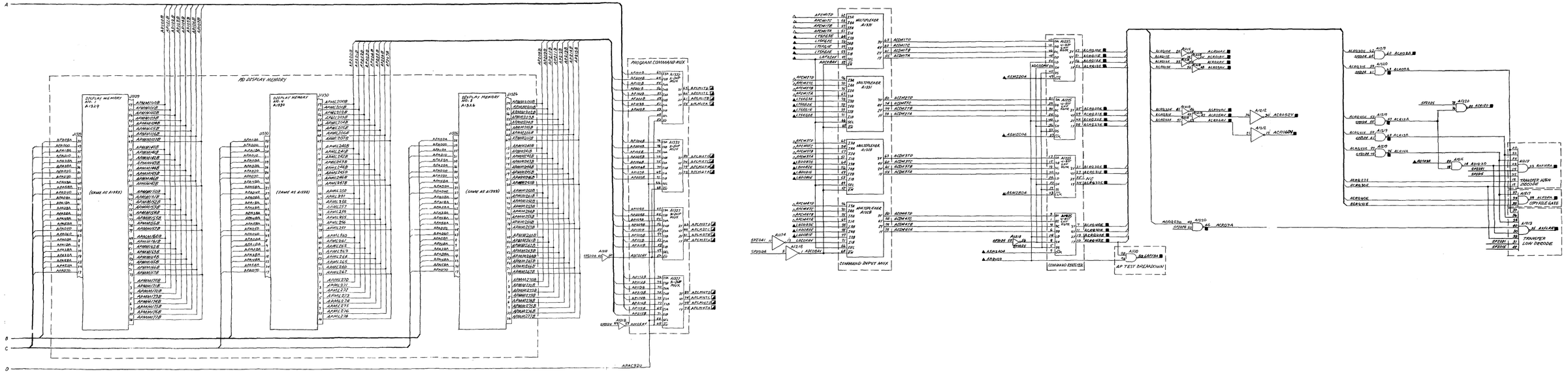
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

MS3901-24

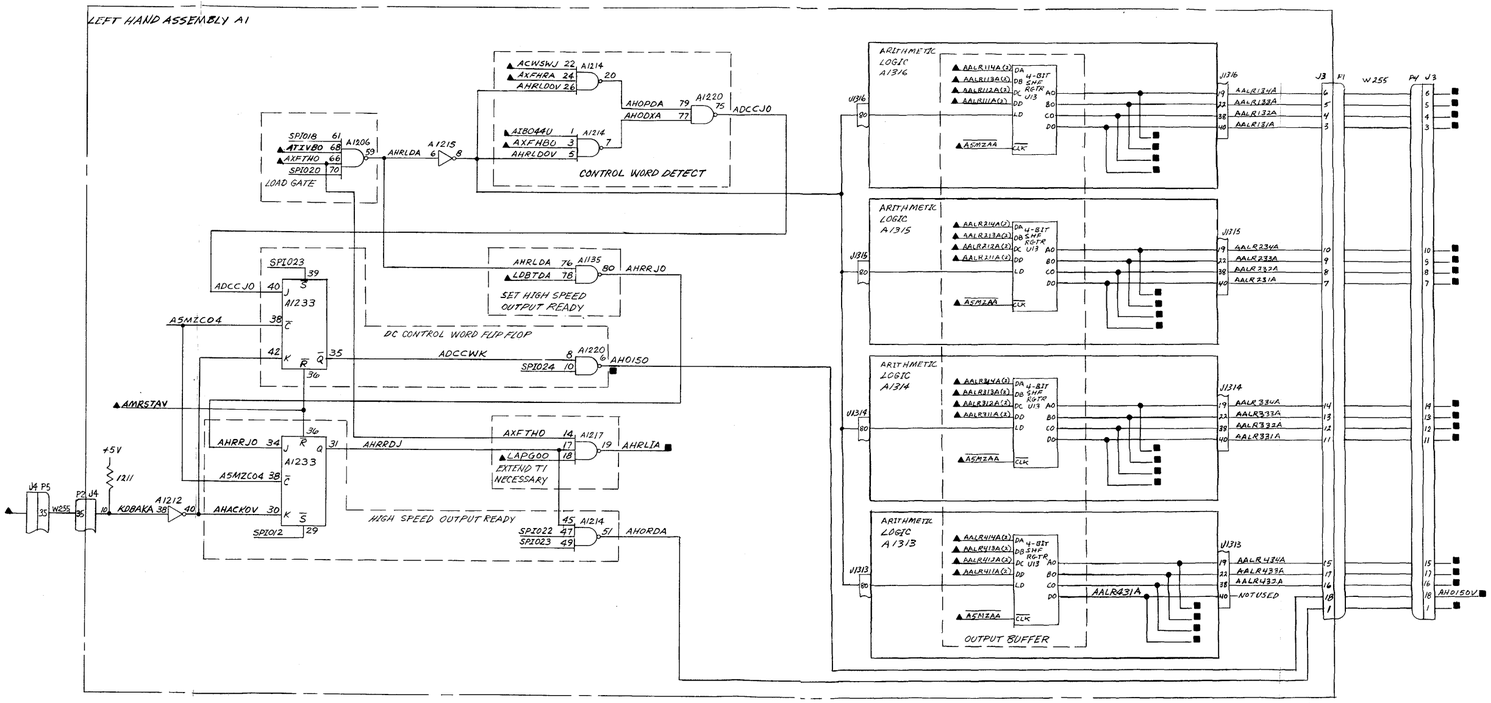
FO-9. Alterable Processor Program Memory and Command Register Logic Diagram (Sheet 1 of 2)


PD DISPLAY MEMORY
DISPLAY MEMORY ADR. 1 A1329
DISPLAY MEMORY ADR. 2 A1330
DISPLAY MEMORY ADR. 3 A1326
(SAME AS A1330)
(SAME AS A1329)
PROGRAM COMMAND MUX
A1327 2-INPUT MUX
MULTIPLEXER A1331
MULTIPLEXER A1332
MULTIPLEXER A1333
COMMAND INPUT MUX
COMMAND REGISTER
A1335 4-BIT REGISTER
A1336 4-BIT REGISTER
A1337 4-BIT REGISTER
A1338
A1339
A1340
A1341
A1342
A1343
A1344
A1345
A1346
A1347
A1348
A1349
A1350
A1351
A1352
A1353
A1354
A1355
A1356
A1357
A1358
A1359
A1360
A1361
A1362
A1363
A1364
A1365
A1366
A1367
A1368
A1369
A1370
A1371
A1372
A1373
A1374
A1375
A1376
A1377

INPUTS	F/O - SH
AALR111A	8-1
AALR112A	8-1
AALR113A	8-1
AALR114A	8-1
AALR211A	8-1
AALR212A	8-1
AALR213A	8-1
AALR214A	8-1
AALR311A	8-2
AALR312A	8-2
AALR313A	8-2
AALR314A	8-2
AALR411A	8-2
AALR412A	8-2
AALR413A	8-2
AALR414A	8-2
ACWSWJ	13-0
AIB044U	2-0
AMRSTAV	53-0
ATIVB0	14-2
AXFTH0	14-1
$\overline{\text{ASMZAA}}$	6-2
ASMZC04	54-2
KDBAKA	28-0
LAPG00	49-0
LDBTDA	49-0

OUTPUTS	F/O - SH
AALR432A	6-3
	30-1
AALR433A	6-3
	30-1
AALR434A	6-3
	30-1
AH0RDA	28-0
AH0150V	30-1
AHRLIA	49-0
	14-2

OUTPUTS	F/O - SH
AALR131A	6-2
	30-1
AALR132A	6-2
	30-1
AALR133A	6-2
	30-1
AALR134A	6-2
	30-1
AALR231A	6-2
	30-1
AALR232A	6-2
	30-1
AALR233A	6-2
	30-1
AALR234A	6-2
	30-1
AALR331A	6-2
	30-1
AALR332A	6-2
	30-1
AALR333A	6-2
	30-1
AALR334A	6-2
	30-1
AALR431A	6-3
	30-1



MS200126

FO-10. Alterable Processor High Speed Output Buffer Logic Diagram

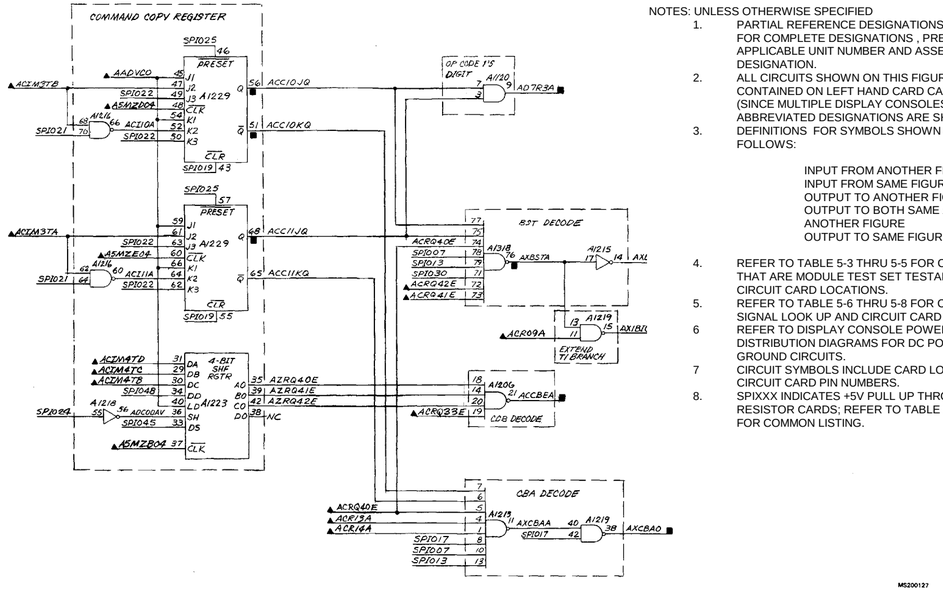
NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   INPUT FROM ANOTHER FIGURE
   INPUT FROM SAME FIGURE
   OUTPUT TO ANOTHER FIGURE
   OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

INPUTS	F/O - SH	OUTPUTS	F/O - SH
AADVC0	12-0	ACCBEA	15-0
ASMZB04	54-2	ACC10QQ	8-2
ASMZD04	54-2		14-1
ASMZE04	54-2		02-1
ACIM3TA	9-2	ACC10NQ	14-0
ACIM3TB	9-2	ACC11QQ	8-2
ACIM4TB	0-2		14-1
ACIM47C	9-2	AD7R3A	9-2
ACIM47D	9-2	AXBSTA	7-1
ACR09A	9-2		0-1
ACR13A	9-2		15-0
ACR14A	9-2	AXBST0V	14-1
ACRQ33E	9-2	AXCBA0	0-1
ACRQ40E	9-2	AX11B10	7-1
ACRQ41E	9-2		14-2
ACRQ42E	9-2		



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

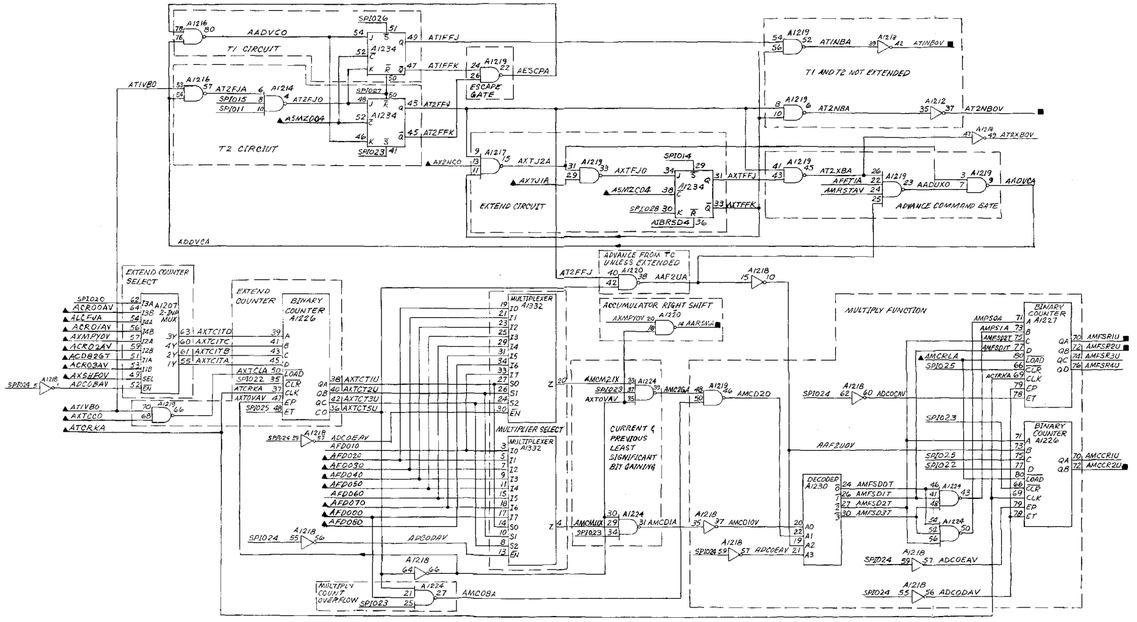
   INPUT FROM ANOTHER FIGURE
   INPUT FROM SAME FIGURE
   OUTPUT TO ANOTHER FIGURE
   OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

MS200127

FO-11. Alterable Processor Timing and Control Command Copy Register Logic Diagram

INPUTS	F/O - SH	OUTPUTS	F/O - SH
AAFT1A	14-2	AADVCA	5-0
ASMZC04	54-2		9-1
ASMZD04	54-2	AADVCO	4-1
ACD026T	14-1		9-2
ACR00AV	9-2		11-0
ACR01AV	9-2	AARSMA	6-1
ACR02AV	9-2	AMCCR1U	6-1
ACR03AV	9-2	AMCCR2U	6-1
AFD000	7-2	AMFSR1U	6-1
AFD010	7-2	AMFSR2U	6-1
AFD020	7-2	AMFSR3U	6-1
AFD030	7-2	AMFSR4U	6-1
AFD040	7-2	AT1FFJ	14-2
AFD050	7-2	AT2FFJ	5-0
AFD060	7-2		6-1
AFD070	7-2		14-2
AFD080	7-2	AT1NB0V	14-2
			15-0
ALCV3A	14-2	AT2NB0V	14-1
AMCR1A	14-2	AT2XB0A	15-0
AMRSTAV	55-0	AT2XB0V	14-2
ATCRKA	54-2		
AT1VB0	14-2		
AXT2NC0	14-2		
AXMPY0V	14-2		
AXSHF0V	14-1		
AXTCC0	14-2		
AXT31A	14-4		



NOTES: UNLESS OTHERWISE SPECIFIED

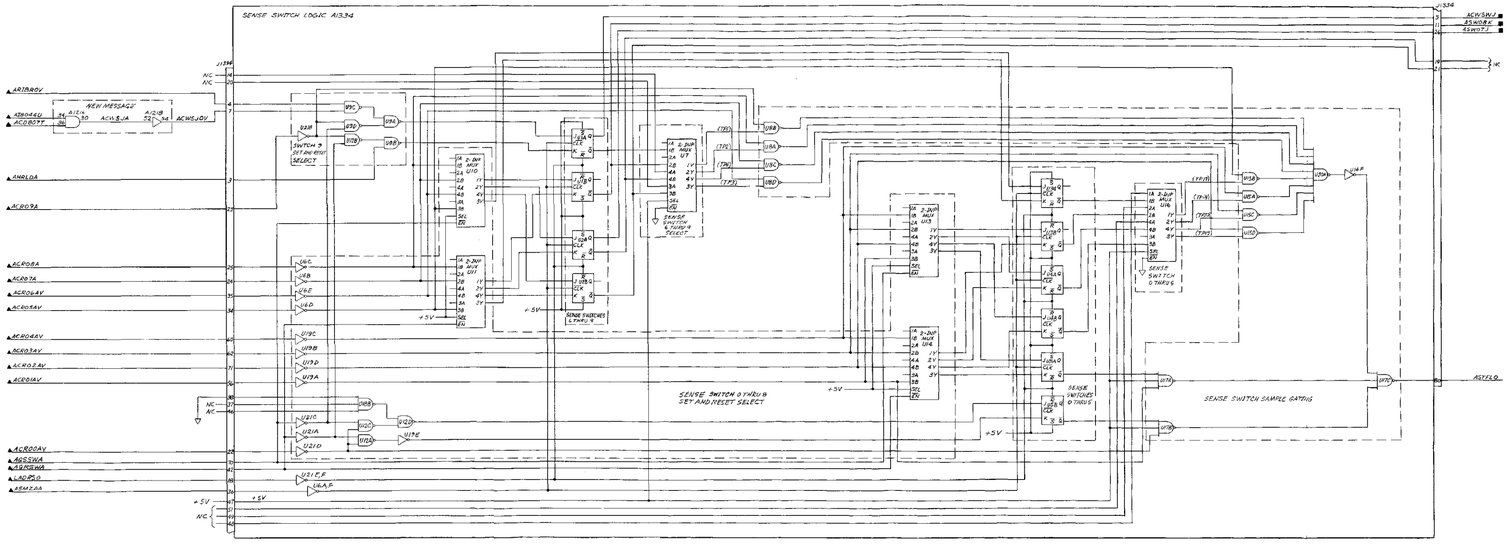
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   INPUT FROM ANOTHER FIGURE
   INPUT FROM SAME FIGURE
   OUTPUT TO ANOTHER FIGURE
   OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6 REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7 CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

MS200128

FO-12. Alterable Processor Timing and Control Command Timing Logic Diagram



NOTES: UNLESS OTHERWISE SPECIFIED

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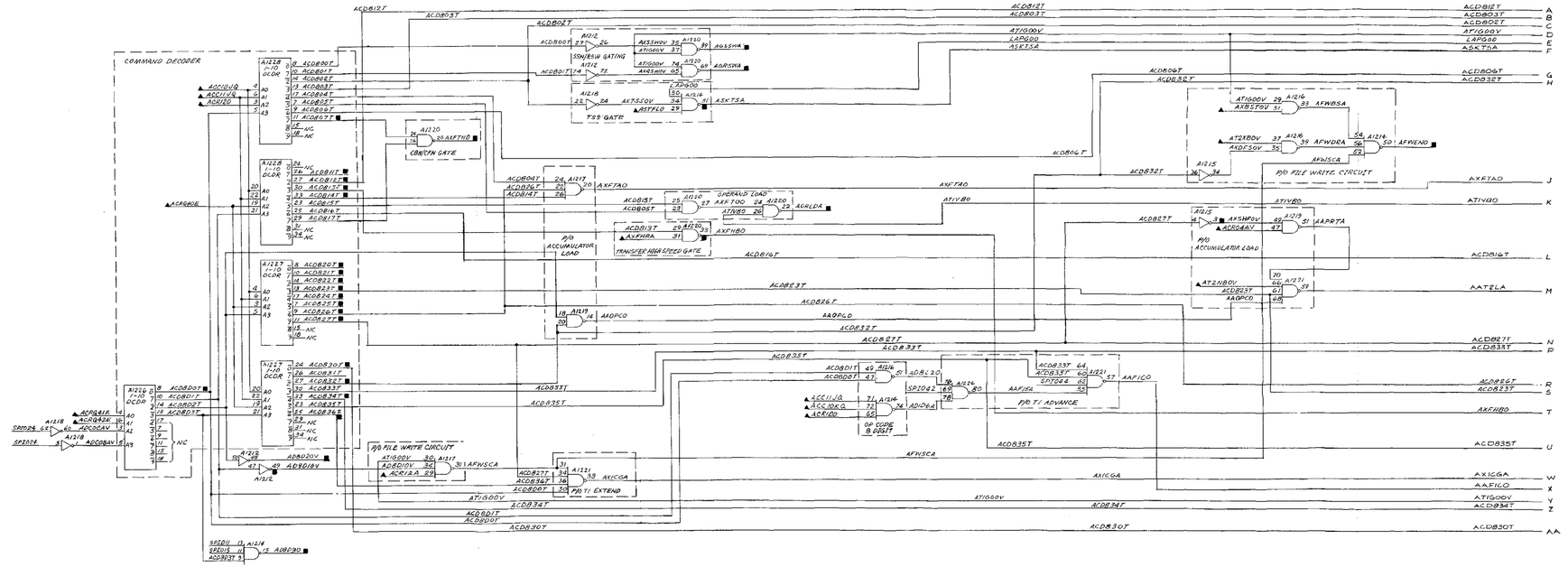
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   INPUT FROM ANOTHER FIGURE
   INPUT FROM SAME FIGURE
   OUTPUT TO ANOTHER FIGURE
   OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6 REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7 CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.

FO-13. Alterable Processor Timing and Control Sense Switch Logic Diagram



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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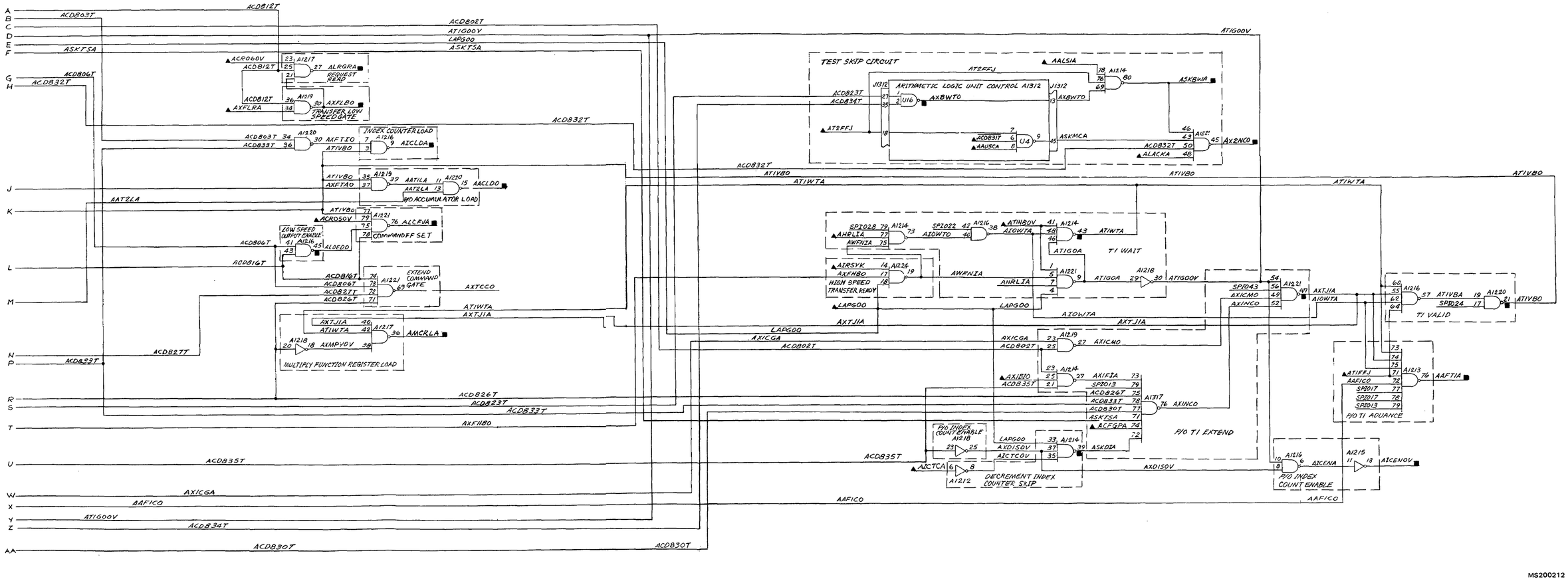
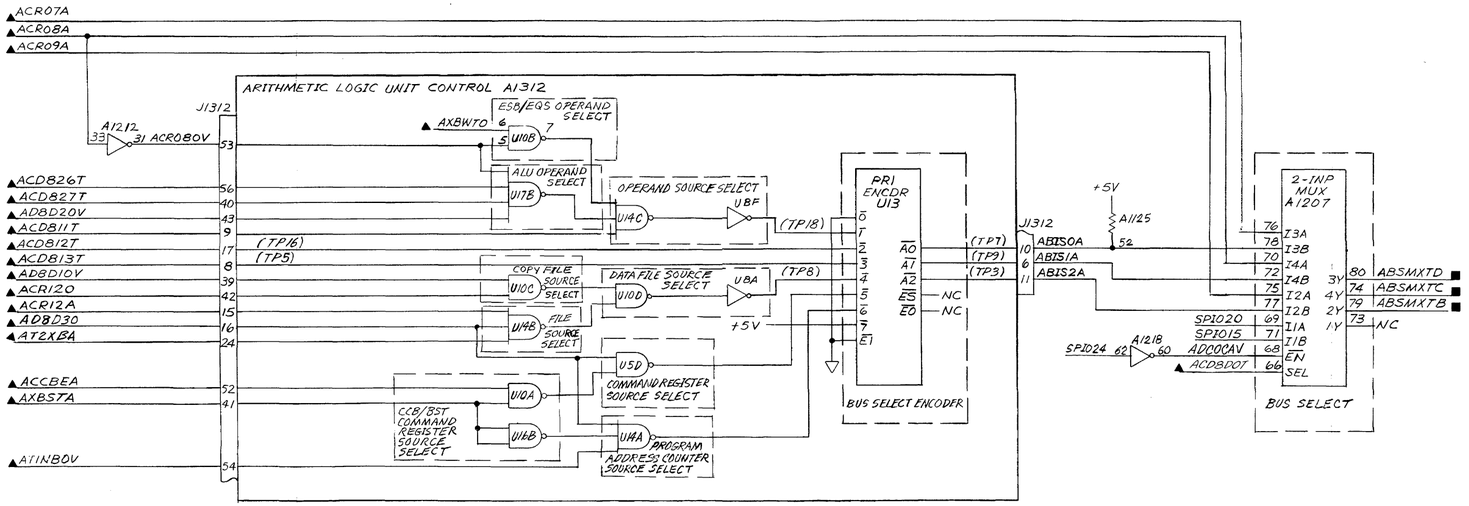
FO-14. Alterable Processor Timing and Control Instruction Decode Logic Diagram (Sheet 1 of 2)



FO-14. Alterable Processor Timing and Control Instruction Decode Logic Diagram (Sheet 2 of 2)

INPUTS	F/O - SH	OUTPUTS	F/O - SH
ACCBEA	11-0	ABSMXTB	8-1
ACD8D0T	14-1		52-2
ACD811T	14-1	ABSMXTC	8-1
ACD812T	14-1		52-2
ACD813T	14-1	ABSMXTD	8-1
ACD826T	14-1		52-2
ACD827T	14-1		
ACR07A	9-2		
ACR08A	9-2		
ACR09A	9-2		
ACR12A	9-2		
ACR120	9-2		
AD8D10V	14-1		
AD8D20V	14-1		
AD8D30	14-1		
AT1NB0V	12-0		
AT2XBA	12-0		
AXBSTA	11-0		
AXBWT0	14-2		



FO-15. Alterable Processor Timing and Control Data Bus Select Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

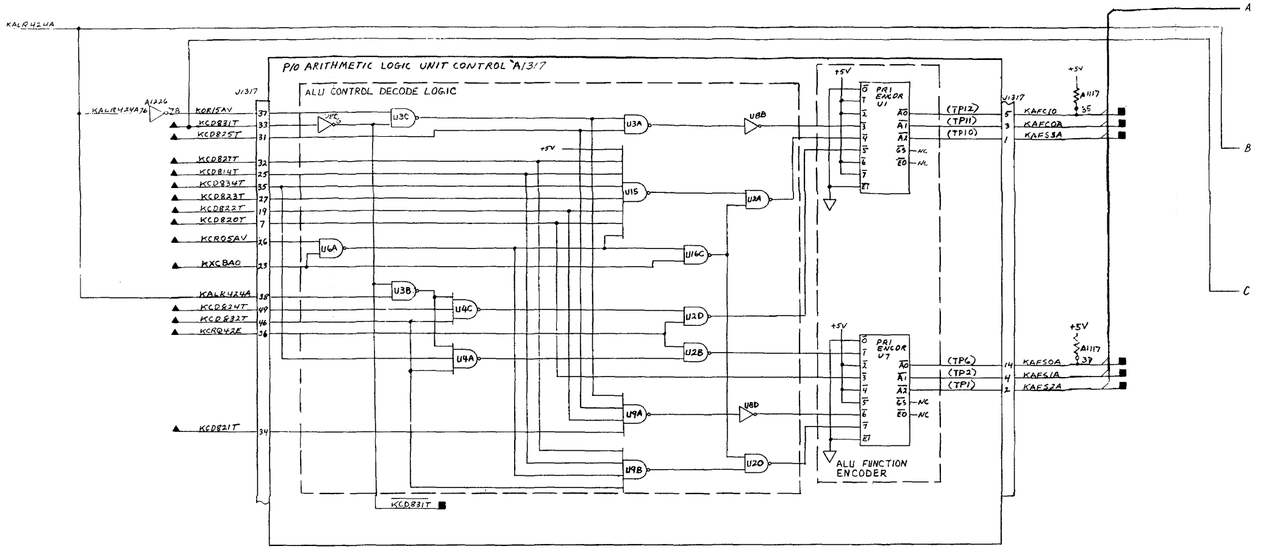
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

INPUTS	F/O - SH	INPUTS	F/O - SH
KACLD0	26-1	KALR411A	18-2
KALR111A	18-1	KALR412A	18-2
KALR112A	18-1	KALR413A	18-2
KALR113A	18-1	KALR414A	18-2
KALR114A	18-1	KALR431A	20-0
KALR131A	20-0	KALR432A	20-0
KALR132A	20-0	KALR433A	20-0
KALR133A	20-0	KALR434A	20-0
KALR134A	20-0	KCD814T	26-1
KALR211A	18-2	KCD820T	26-1
KALR212A	18-2	KCD821T	26-1
KALR213A	18-2	KCD822T	26-1
KALR214A	18-2	KCD823T	26-1
KALR231A	20-0	KCD824T	26-1
KALR232A	20-0	KCD825T	26-1
KALR233A	20-0	KCD827T	26-1
KALR234A	20-0	KCD831T	26-1
KALR311A	18-2	KCD832T	26-1
KALR312A	18-2	KCD834T	26-1
KALR313A	18-2	KCR07A	19-2
KALR314A	18-2	KCR05AV	19-2
KALR331A	20-0	KCRQ20E	19-2
KALR332A	20-0	KCRQ21E	19-2
KALR333A	20-0	KCRQ22E	19-2
KALR334A	20-0	KCRQ42E	19-2

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KAEC0A	52-3	KALR121A	18-1
KAFCI0	52-3	KALR122A	18-1
KAFS0A	52-3	KALR123A	18-1
KAFS1A	52-3	KALR124A	18-1
KAFS2A	52-3	KALR201A	18-2
KAFS3A	52-3	KALR202A	18-2
KALR101A	18-1	KALR203A	18-2
KALR102A	18-1	KALR204A	18-2
KALR103A	18-1	KALR221A	18-2
KALR104A	18-1	KALR222A	18-2

INPUTS	F/O - SH	INPUTS	F/O - SH
KFD000	17-2	KFD140	17-2
KFD010	17-2	KFD150	17-2
KFD020	17-2	KHC1C0	52-2
KFD030	17-2	KHC2C0	52-2
KFD040	17-2	KHC3C0	52-2
KFD050	17-2	KT2FFJ	24-0
KFD060	17-2	KT2SF0	26-2
KFD070	17-2	KXCBA0	23-0
KFD080	17-2	KXSHF0V	26-1
KFD090	17-2	K0RLDA	26-1
KFD100	17-2	K5MZBAH	54-3
KFD110	17-2	LENCB5T	52-2
KFD120	17-2	LHCR3A	52-2
KFD130	17-2		

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KALR223A	18-2	KBM020	52-3
KALR224A	18-2	KBM030	52-3
KALR301A	18-2	$\overline{\text{KCD831T}}$	26-2
KALR302A	18-2	KSKDFA	19-1
KALR303A	18-2	K12130	24-0
KALR304A	18-2	$\overline{\text{K5MZBAH}}$	20-0
KALR321A	18-2		
KALR322A	18-2		
KALR323A	18-2		
KALR324A	18-2		
KALR401A	18-2		
KALR402A	18-2		
KALR403A	18-2		
KALR404A	18-2		
KALR421A	18-2		
KALR422A	18-2		
KALR423A	18-2		
KALR424A	18-2		



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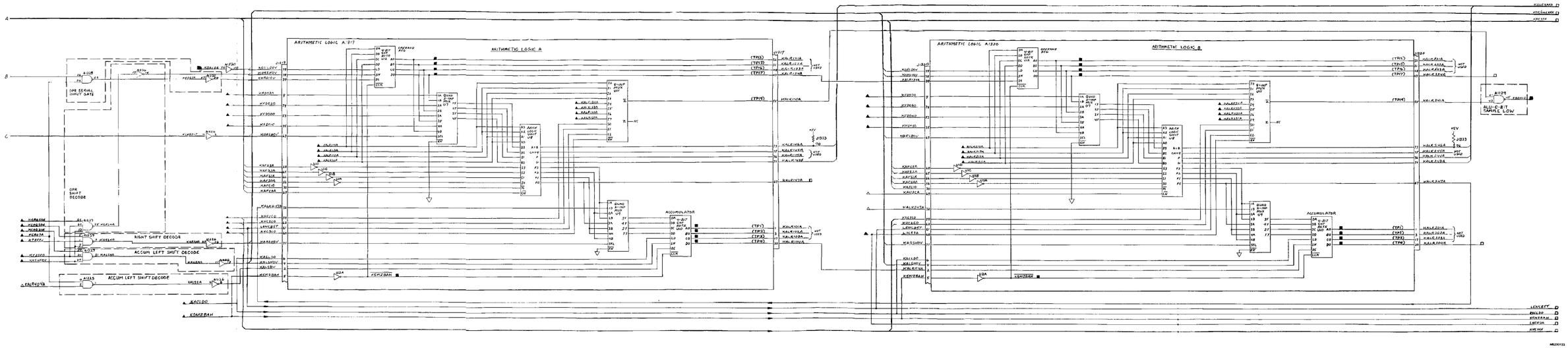
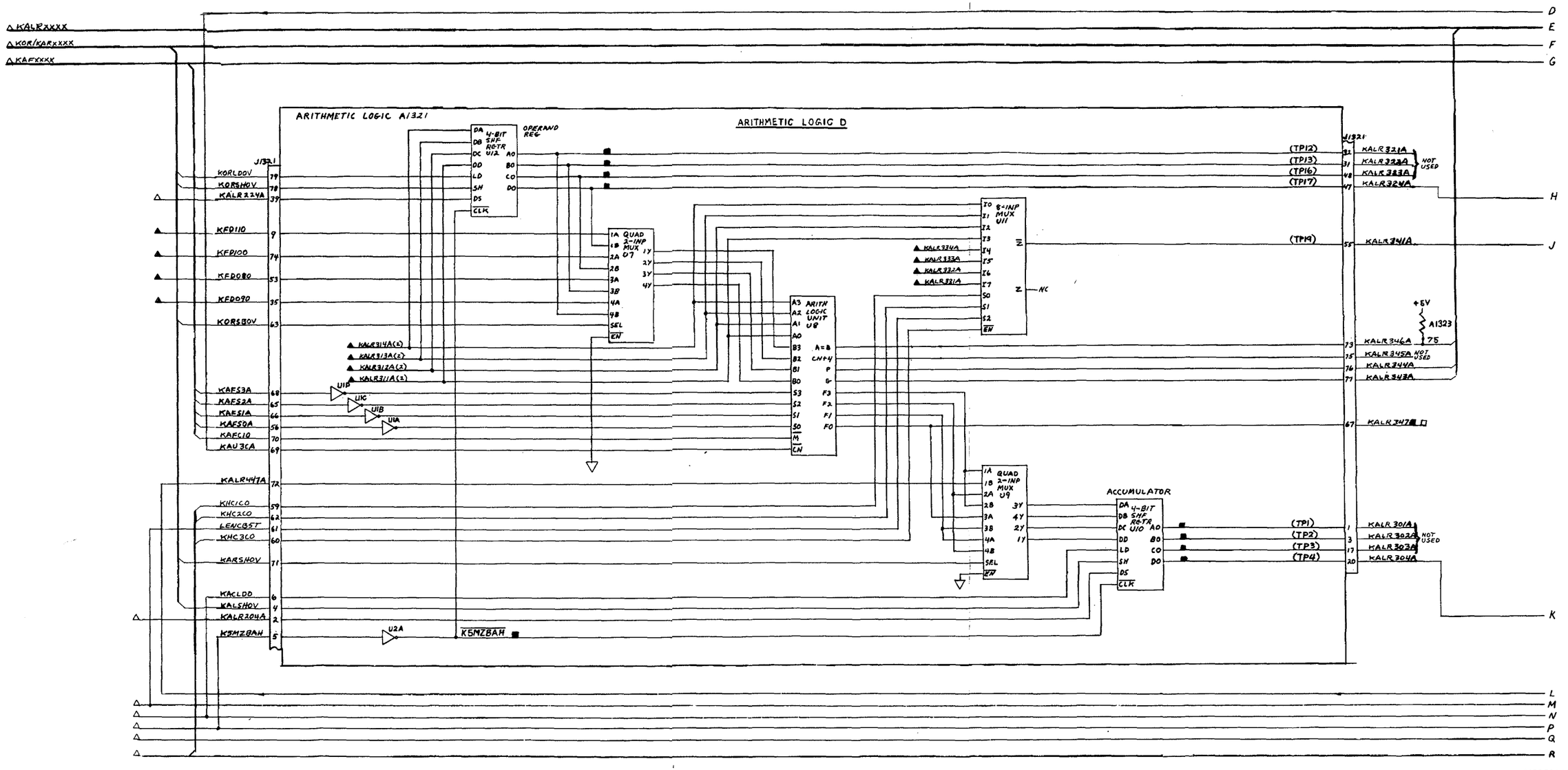
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

FO-16. Display Controller Arithmetic Logic Diagram (Sheet 1 of 4)



FO-16. Display Controller Arithmetic Logic Diagram (Sheet 2 of 4)



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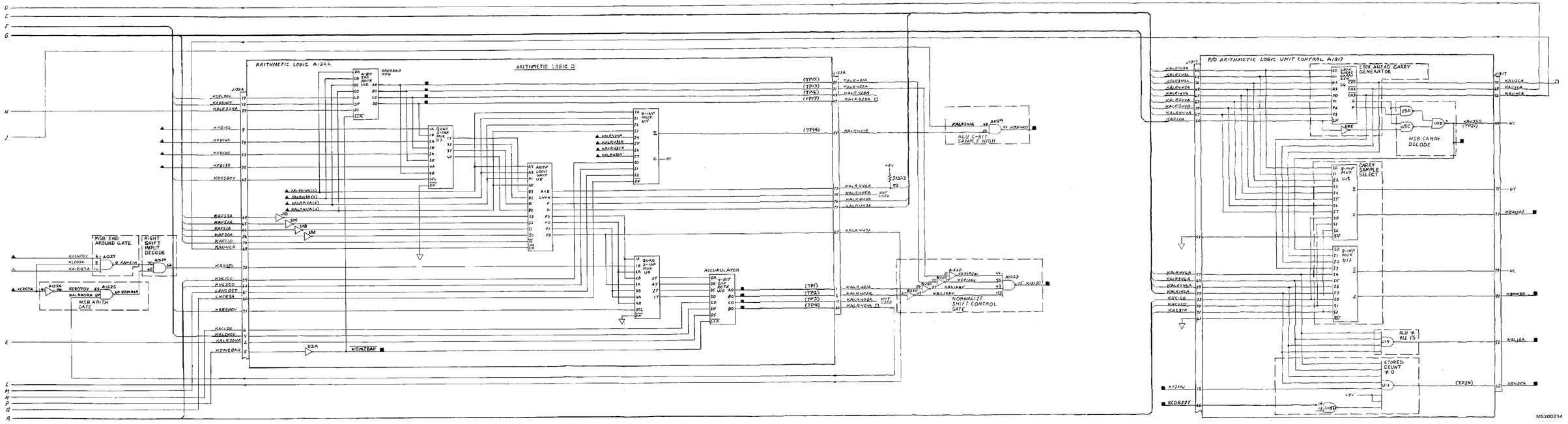
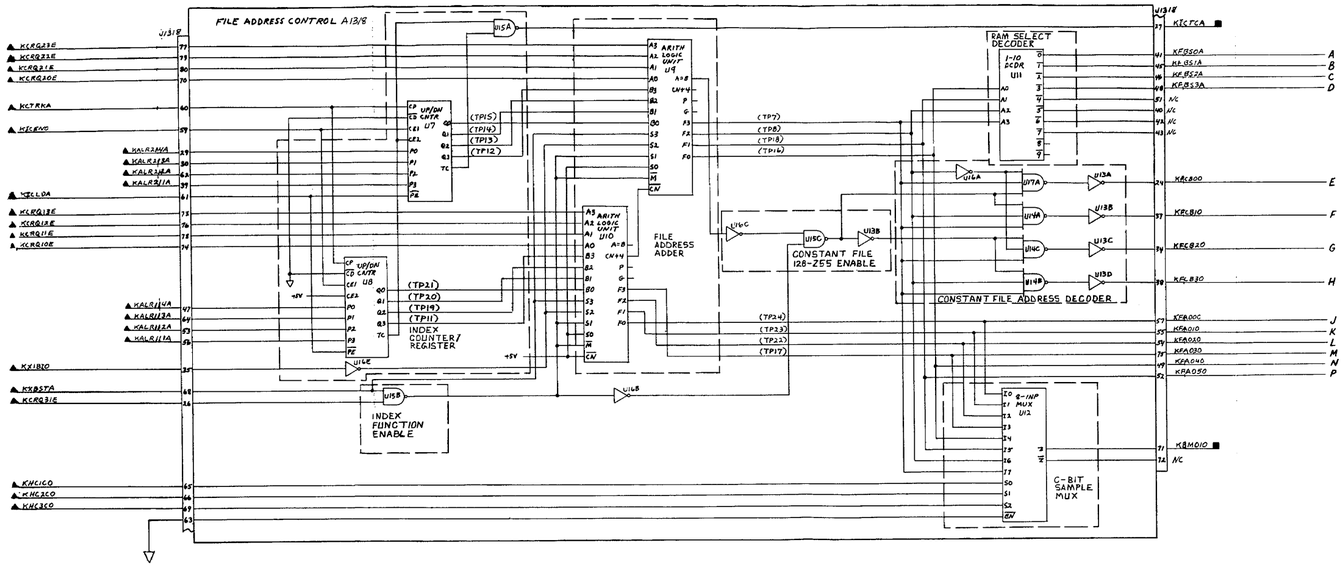
FO-16. Display Controller Arithmetic Logic Diagram (Sheet 3 of 4)



FO-16. Display Controller Arithmetic Logic Diagram (Sheet 4 of 4)

INPUTS	F/O - SH	INPUTS	F/O - SH
KALR111A	18-1	KCRQ13E	19-2
KALR112A	18-1	KCRQ20E	19-2
KALR113A	18-1	KCRQ21E	19-2
KALR114A	18-1	KCRQ22E	19-2
KALR211A	18-2	KCRQ23E	19-2
KALR212A	18-2	KCRQ31E	19-2
KALR213A	18-2	KCTRKA	54-3
KALR214A	18-2	KFWEN0	26-1
KALR311A	18-2	KHC1C0	52-2
KALR312A	18-2	KHC2C0	52-2
KALR313A	18-2	KHC3C0	52-2
KALR314A	18-2	KICEN0	26-2
KALR411A	18-2	KICLDA	26-1
KALR412A	18-2	KMWRK0	54-3
KALR413A	18-2	KXBSTA	23-0
KALR414A	18-2	KXTLSA	23-0
KCBQ10E	19-2	KX1EI0	23-0
KCBQ11E	19-2	KSQFAV	
KCBQ12E	19-2	KSQFAV	

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KBM010	52-3	KFD080	16-3
KFD000	16-2		18-2
	18-1		52-2
	52-2	KFD090	16-3
KFD010	16-2		18-2
	18-1		52-2
	52-2	KFD100	16-3
KFD020	16-2		18-2
	18-1		52-2
	52-2	KFD110	16-3
KFD030	16-2		18-2
	18-1		52-2
	52-2	KFD120	16-4
KFD040	16-2		18-2
	18-2		52-2
	52-2	KFD130	16-4
KFD050	16-2		18-2
	18-2		52-2
	52-2	KFD140	16-4
KFD060	16-2		18-2
	18-2		52-2
	52-2	KFD150	16-4
KFD070	16-2		18-2
	18-2		52-2
	52-2	KICTCA	26-2



FO-17. Display Controller Data File Storage and Address Logic Diagram (Sheet 1 of 2)

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
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4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
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6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
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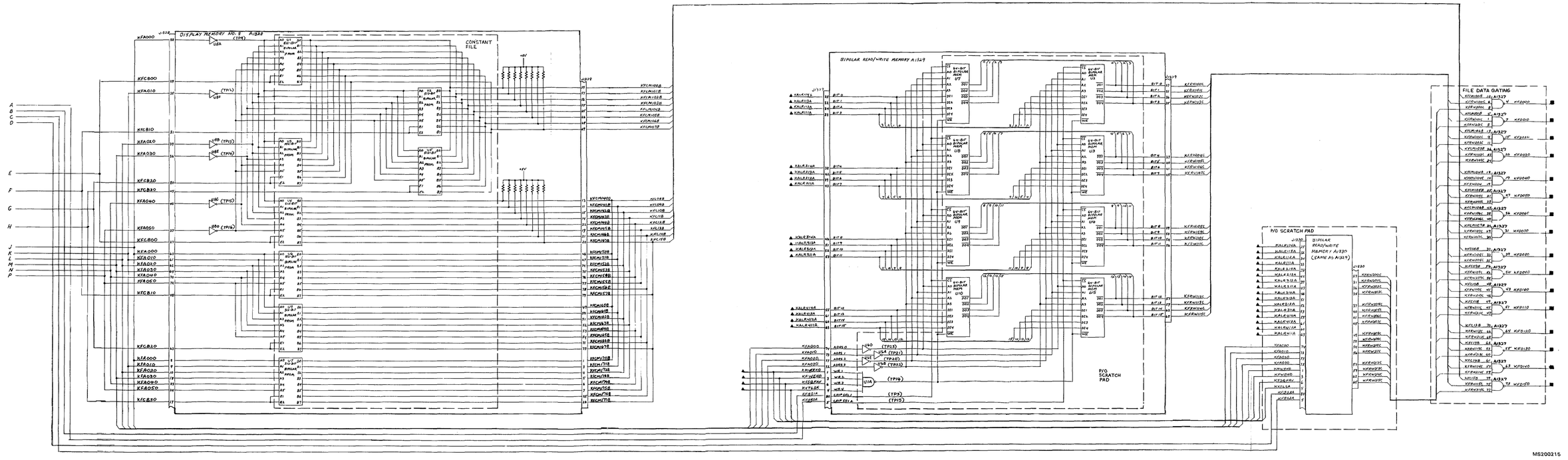
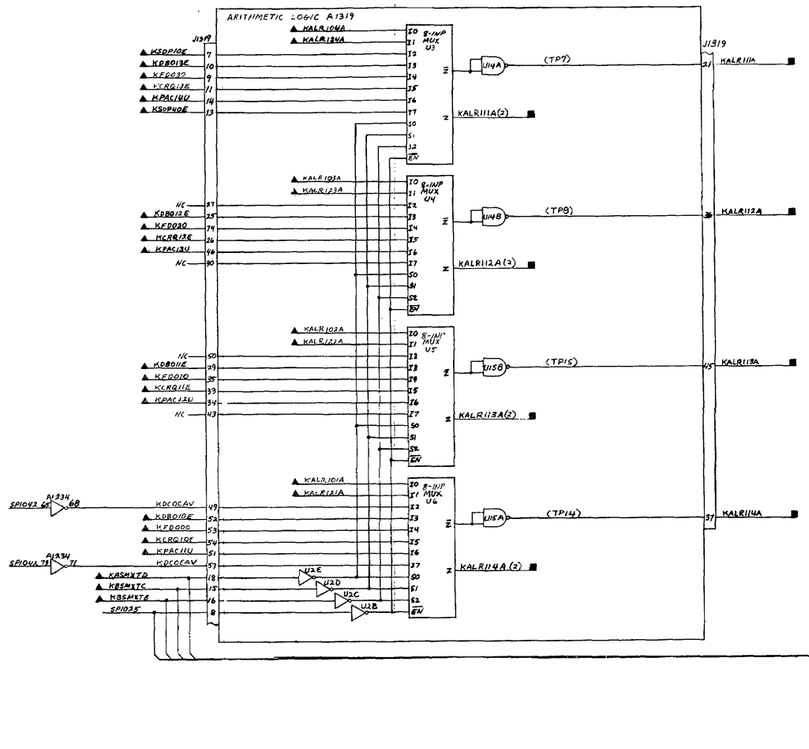


FO-17. Display Controller Data File Storage and Address Logic Diagram (Sheet 2 of 2)

INPUTS	F/O - SH	INPUTS	F/O - SH	INPUTS	F/O - SH	INPUTS	F/O - SH	INPUTS	F/O - SH	INPUTS	F/O - SH
KALR101A	16-2	KALR402A	16-4	KDB010E	30-2	KFD110	17-2	KSDP32E	21-0	KSDP52E	21-0
KALR102A	16-2	KALR403A	16-4	KDB011E	30-2	KFD120	17-2	KSDP33E	21-0	KSDP53E	21-0
KALR103A	16-2	KALR404A	16-4	KDB012E	30-2	KFD130	17-2	KSDP40E	21-0	KSDP60E	21-0
KALR104A	16-2	KALR421A	16-4	KDB020E	30-2	KFD140	17-2	KSDP41E	21-0	KSDP61E	21-0
KALR121A	16-2	KALR422A	16-4	KDB021E	30-2	KFD150	17-2	KSDP42E	21-0	KSDP62E	21-0
KALR122A	16-2	KALR423A	16-4	KDB022E	30-2	KPAC11U	19-1	KSDP43E	21-0	KSDP63E	21-0
KALR123A	16-2	KALR424A	16-4	KDB023E	30-2	KPAC12U	19-1	KSDP50E	21-0	KSPCSJ	21-0
KALR124A	16-2	KBSMXTB	27-0	KDB030E	30-2	KPAC13U	19-1	KSDP51E	21-0		
KALR201A	16-2	KBSMXTC	27-0	KDB031E	30-2	KPAC14U	19-1				
KALR202A	16-2	KBSMXTD	27-0	KDB032E	30-2	KPAC21U	19-1				
KALR203A	16-2	KCRQ10E	19-2	KDB033E	30-2	KPAC22U	19-1				
KALR204A	16-2	KCRQ11E	19-2	KDB040E	30-2	KPAC23U	19-1				
KALR221A	16-2	KCRQ12E	19-2	KDB041E	30-2	KPAC24U	19-1				
KALR222A	16-2	KCRQ13E	19-2	KDB042E	30-2	KPAC31U	19-1				
KALR223A	16-2	KCRQ20E	19-2	KFD000	17-2	KPAC32U	19-1				
KALR224A	16-2	KCRQ21E	19-2	KFD010	17-2	KSDP10E	21-0				
KALR301A	16-3	KCRQ22E	19-2	KFD020	17-2	KSDP11E	21-0				
KALR302A	16-3	KCRQ23E	19-2	KFD030	17-2	KSDP12E	21-0				
KALR303A	16-3	KCRQ30E	19-2	KFD040	17-2	KSDP13E	21-0				
KALR304A	16-3	KCRQ31E	19-2	KFD050	17-2	KSDP20E	21-0				
KALR321A	16-3	KCRQ41E	19-2	KFD060	17-2	KSDP21E	21-0				
KALR322A	16-3	KCRQ42E	19-2	KFD070	17-2	KSDP22E	21-0				
KALR323A	16-3	KCRQ43E	19-2	KFD080	17-2	KSDP23E	21-0				
KALR324A	16-3	KCR100V	23-0	KFD090	17-2	KSDP30E	21-0				
KALR401A	16-4	KCR110V	23-0	KFD100	17-2	KSDP31E	21-0				
		KCR120	19-2								

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH	OUTPUTS	F/O - SH	OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KALR111A	17-1	KALR114A	17-1	KALR213A	17-1	KALR312A	17-2	KALR411A	17-2
	19-1		19-1		19-1		19-1		20-0
	22-0		22-0		20-0		20-0		16-4
	20-0		20-0		16-2		16-3	KALR412A	17-2
	16-2		16-2	KALR214A	17-1	KALR313A	17-2		20-0
KALR112A	17-1	KALR211A	17-1		19-1		19-1		16-4
	19-1		19-1		22-0		22-0	KALR413A	17-2
	22-0		20-0		20-0		20-0		20-0
	20-0		16-2		16-2		16-3		16-4
	16-2	KALR212A	17-1	KALR311A	17-2	KALR314A	17-2	KALR414A	17-2
KALR113A	17-1		19-1		19-1		19-1		20-0
	19-1		22-0		20-0		22-0		16-4
	22-0		20-0		16-3		20-0		
	20-0		16-2		16-2				
	16-2								



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FO-18. Display Controller 8-Input Multiplexer Logic Diagram (Sheet 1 of 2)

NOTES: UNLESS OTHERWISE SPECIFIED

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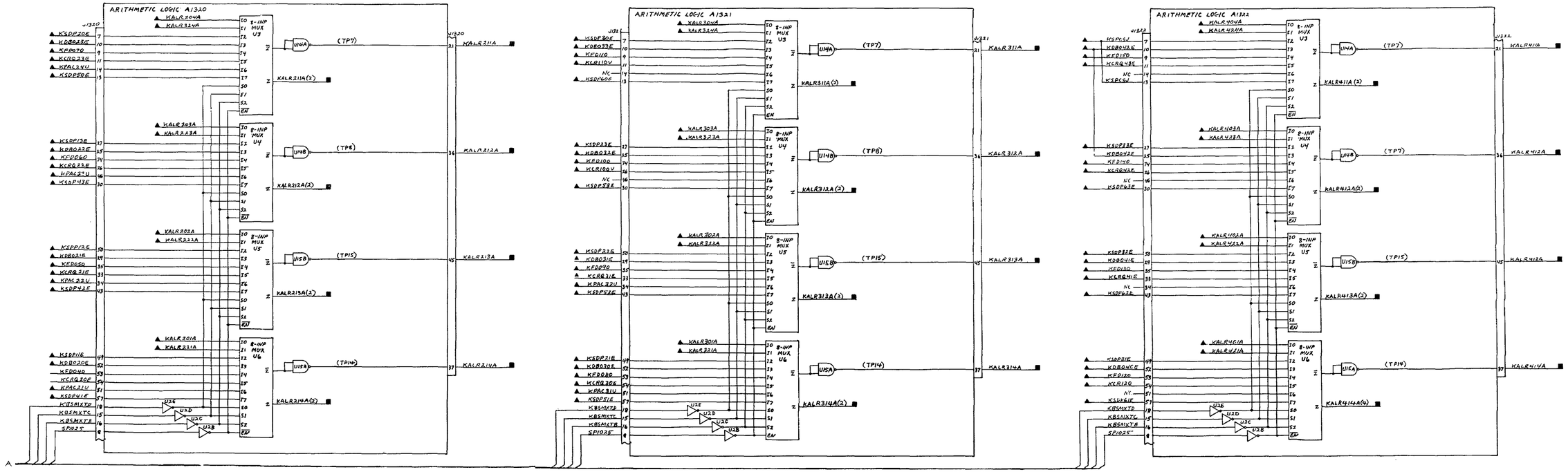

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FO-18. Display Controller 8-Input Multiplexer Logic Diagram (Sheet 2 of 2)

INPUTS	I/O - I30
KADVCA	24-0
KADVCO	24-0
KAIR111A	16-1
KAIR112A	14-1
KAIR113A	16-1
KAIR114A	16-1
KAIR211A	16-1
KAIR212A	16-2
KAIR213A	16-2
KAIR214A	16-2
KAIR311A	16-2
KAIR312A	16-2
KAIR313A	16-2
KAIR314A	16-2
KCD450T	29-1
KCD460T	29-1
KC198KA	54-3
KMRFT84	53-2
KSKBWA	26-2
KSKDFA	16-4
KSKOA	29-2
KSKUCA	24-2

INPUTS	I/O - I31
KM2M28A	23-0
KM2M28B	23-0
KCM147B	23-0
KCM141C	23-0
KC1947D	23-0
KCFIGPA	20-2
KCRQ19E	17-1
	18-2
	20-1
	22-0
	20-1
	22-3
KCRQ11E	17-1
	18-1
	21-0
	22-3
KCRQ12E	17-1
	18-1
	22-0
	22-3
KCRQ13E	17-1
	18-1
	22-0

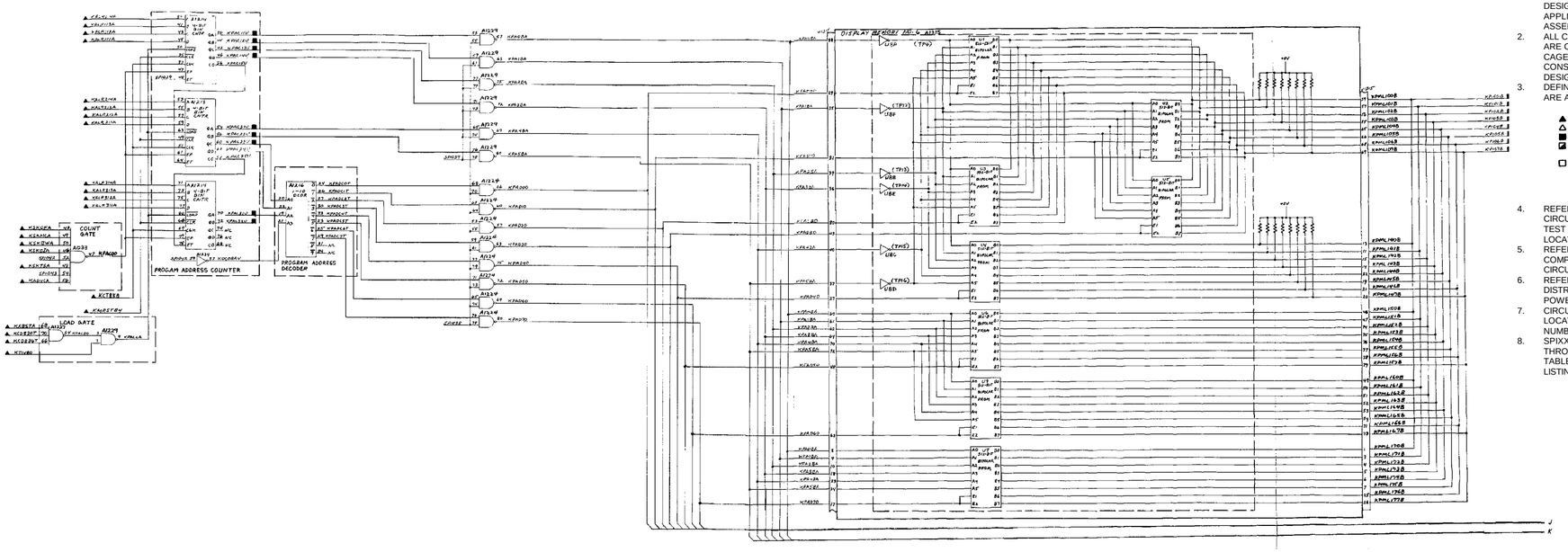
OUTPUTS	I/O - I32
KCRQ19E	17-1
	18-2
	22-3
KCRQ20E	22-3
KCRQ28E	23-0
	23-1
KCRQ48E	26-1
	26-2
KCRQ49E	26-2
	26-3
KCRQ50E	26-3
	27-0
	27-1
KCRQ51E	27-2
	27-3
KCR804V	28-0
	28-1
	27-3

INPUTS	I/O - I33
KCM147A	23-0
KCM141B	23-0
KCM147B	23-0
KCM141C	23-0
KC1947D	23-0
KCFIGPA	20-2
KCRQ19E	17-1
	18-2
	20-1
	22-0
	20-1
	22-3
KCRQ11E	17-1
	18-1
	21-0
	22-3
KCRQ12E	17-1
	18-1
	22-0
	22-3
KCRQ13E	17-1
	18-1
	22-0

OUTPUTS	I/O - I34
KCR804V	28-0
	28-1
KC1947V	24-0
	24-1
KC1948V	25-1
	25-2
KC1949V	25-2
	25-3
KC1950V	25-3
	26-1

OUTPUTS	I/O - I35
KCR13A	22-0
KCR14A	22-0
KCR120	18-2
	23-0
	28-1
	27-0
KDCT3A	48-2
KXFMR4	28-1
KPAC112C	18-1
	53-3
KPAC122U	18-1
	53-3
KPAC123C	18-1
	53-3
KPAC124U	18-1
	53-3
KPAC125U	18-2
	53-3
KPAC126U	18-2
	53-3

OUTPUTS	I/O - I36
KPAC124C	18-1
	53-3
KPAC125U	18-2
	53-3
KP100D	53-3
KP101B	53-3
KP102B	53-3
KP103B	53-3
KP104B	53-3
KP105B	53-3
KP106B	53-3
KP107B	53-3
KP108B	53-3
KP109B	53-3
KP110B	53-3
KP111B	53-3
KP112D	53-3
KP113B	53-3
KP115B	53-3



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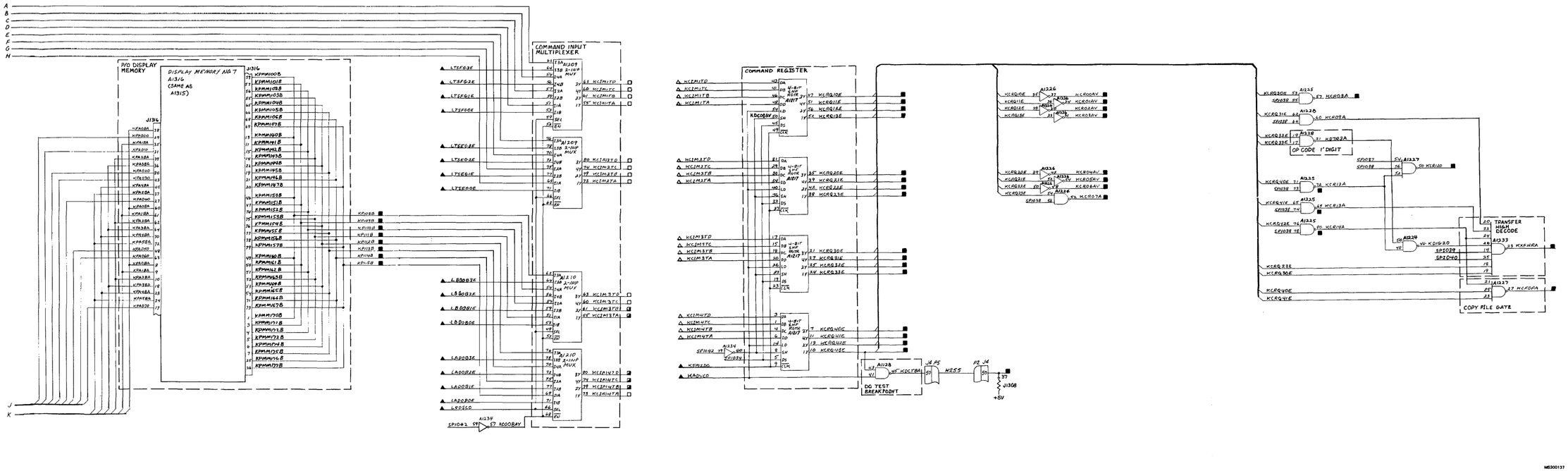
FO-19. Display Controller Program Memory and Command Register Logic Diagram (Sheet 1 of 2)



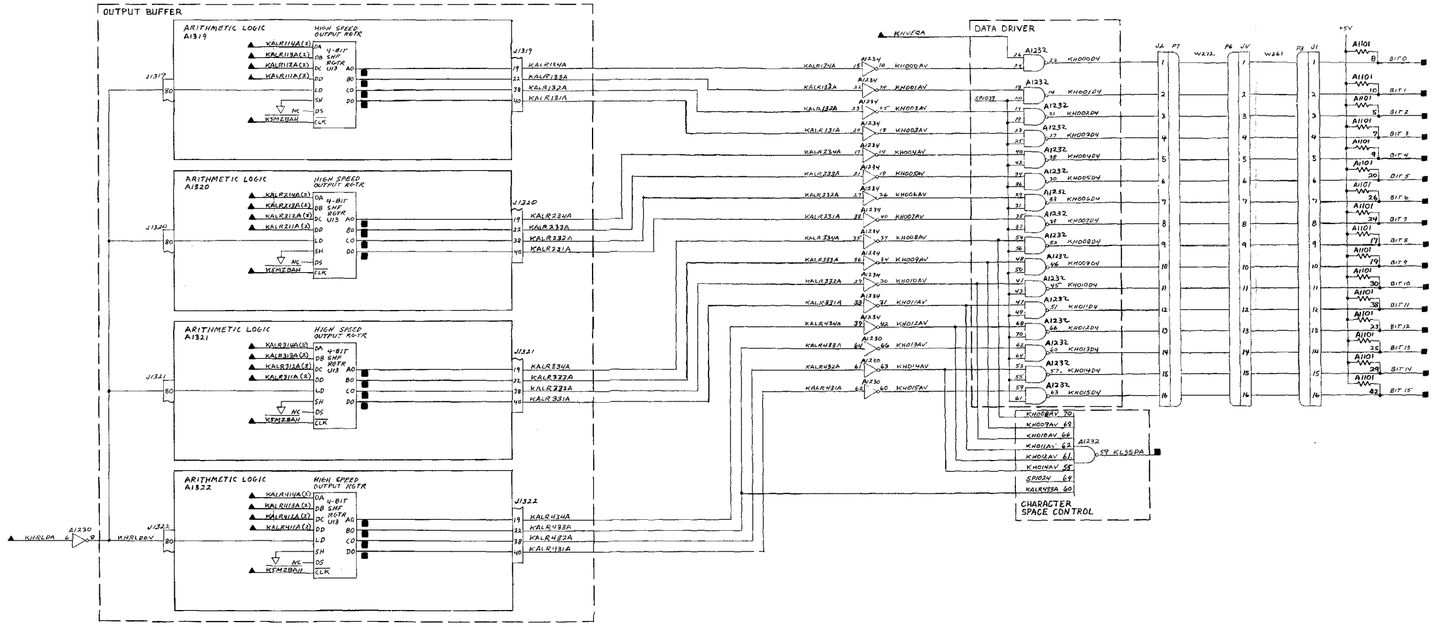
FO-19. Display Controller Program Memory and Command Register Logic Diagram (Sheet 2 of 2)

INPUTS	F/O - SH	INPUTS	F/O - SH
KALR111A	16-1	KALR313A	16-2
KALR112A	16-1	KALR314A	16-2
KALR113A	16-1	KALR411A	16-2
KALR114A	16-1	KALR412A	16-2
KALR211A	16-2	KALR413A	16-2
KALR212A	16-2	KALR414A	16-2
KALR213A	16-2	KHRLDA	26-2
KALR214A	16-2	KHVEQA	22-0
KALR311A	16-2	KSMZBAH	16-2
KALR312A	16-2		

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KH1010D4	37-1	KH1015D4	37-1
	37-2		39-2
	37-3		40-1
	38-2	KLSSFA	22-0
	39-2	KH1008D4	37-1
KH1011D4	37-1		37-2
	37-2		37-3
	37-3		39-2
	38-2	KH1012D4	37-1
	39-2		37-2
KH1012D4	37-1		37-3
	37-2		39-2
	37-3	KH1002D4	37-1
	38-2		37-2
	39-2		37-3
KH1013D4	37-1		39-2
	37-2	KH1003D4	37-1
	37-3		37-2
	38-2		37-3
	39-2		39-2
KH1014D4	37-1	KH1004D4	37-1
	37-2		37-2
	40-1		37-3
	39-2		39-2
	39-2		

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KALR131A	16-2	KALR431A	16-4
KALR132A	16-2	KALR432A	16-4
KALR133A	16-2	KALR433A	16-4
KALR134A	16-2	KALR434A	16-4
KALR231A	16-2	KN0030D4	37-1
KALR232A	16-2		37-2
KALR233A	16-2		37-3
KALR234A	16-2		38-2
KALR331A	16-3		39-2
KALR332A	16-3		
KALR333A	16-3		
KALR334A	16-3		

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
KH1005D4	37-1	KH1007D4	37-1
	37-2		37-2
	37-3		37-3
	39-2		38-2
KH1006D4	37-1	KH1004D4	37-1
	37-2		37-2
	37-3		37-3
	39-2		38-2



FO-20. Display Controller High Speed Output Buffer Logic Diagram.

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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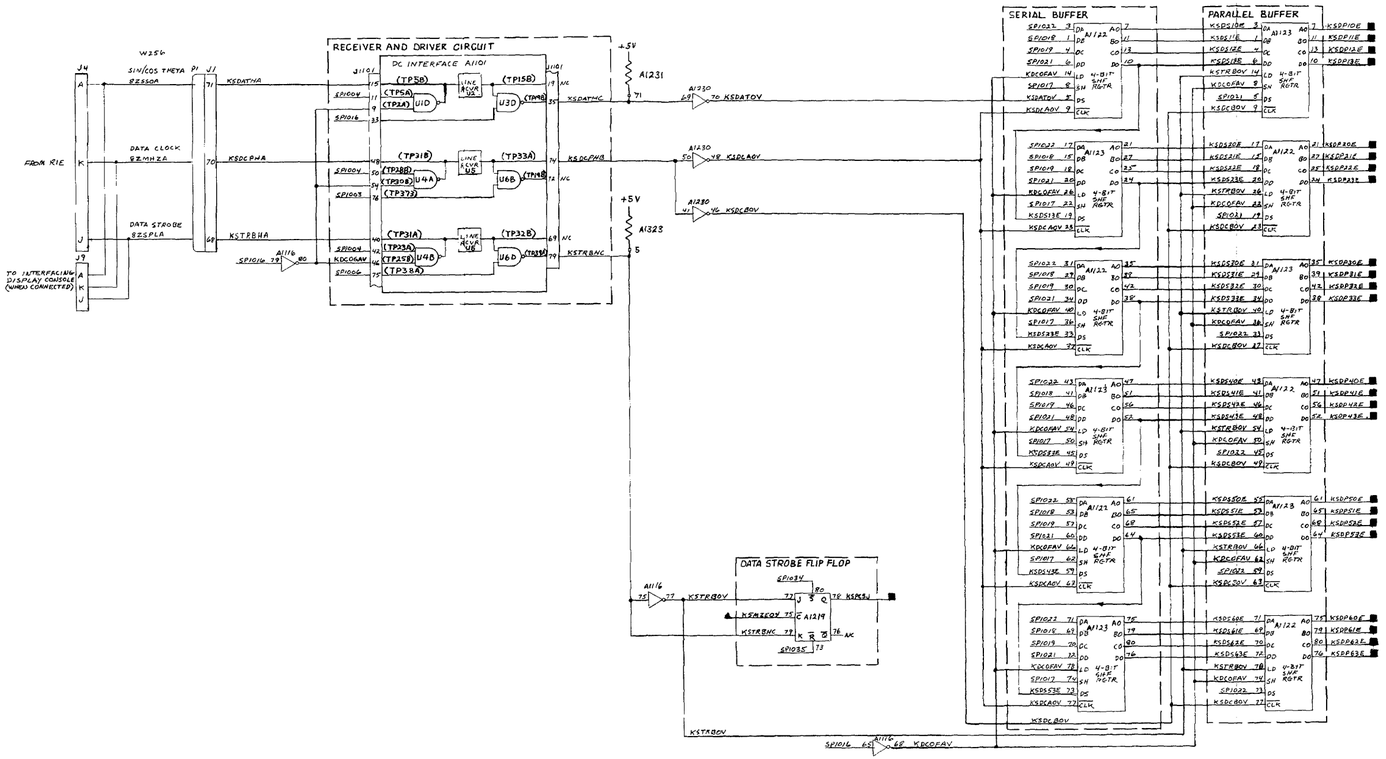
INPUTS	F/O-SH	OUTPUTS	F/O-SH
K5MZE04	54-3	K5DP10E	18-1
		K5DP11E	18-2
		K5DP12E	18-2
		K5DP13E	18-2
		K5DP20E	18-2
		K5DP21E	18-2
		K5DP22E	18-2
		K5DP23E	18-2
		K5DP30E	18-2
		K5DP31E	18-2
		K5DP32E	18-2
		K5DP33E	18-2
		K5DP40E	18-1
		K5DP41E	18-2
		K5DP42E	18-2
		K5DP43E	18-2
		K5DP50E	18-2
		K5DP51E	18-2
		K5DP52E	18-2
		K5DP53E	18-2
		K5DP60E	18-2
		K5DP61E	18-2
		K5DP62E	18-2
		K5DP63E	18-2



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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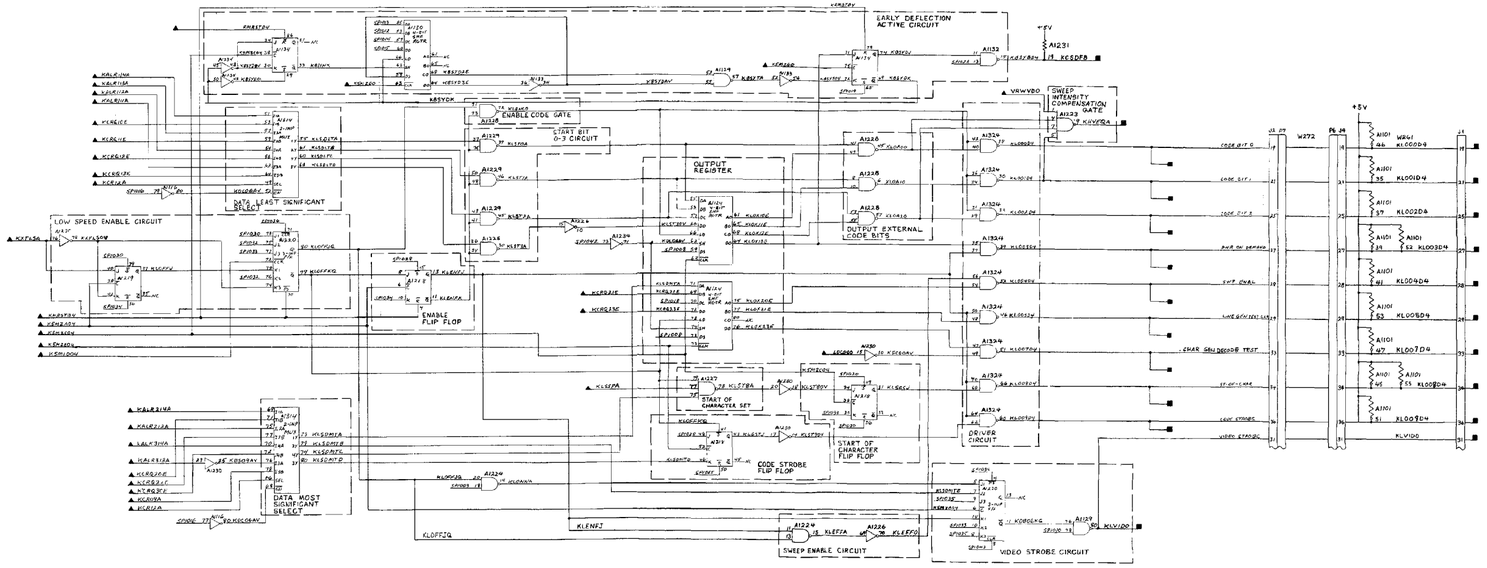
FO-21. Display Controller Serial to Parallel Buffer Logic Diagram.

INPUTS	F/O-SH	INPUTS	F/O-SH
KALR111A	18-1	KMEE04	54-3
KALR112A	18-1	KM12G6	54-3
KALR113A	18-1	LDCC06	49-6
KALR114A	18-1	RMRSTD4	53-6
KALR12A	18-2	VRWVD0	34-1
KALR13A	18-2		
KALR14A	18-2		
KALR15A	18-2		
KALR16A	18-2		
KALR17A	18-2		
KALR18A	18-2		
KALR19A	18-2		
KCBQ10E	18-2		
KCBQ11E	18-2		
KCBQ12E	18-2		
KCBQ13E	18-3		
KCBQ20E	18-3		
KCBQ21E	18-3		
KCBQ22E	18-2		
KCBQ23E	18-2		
KCBQ30E	18-2		
KCBS10A	18-2		
KCB112A	18-2		
KLSSFA	20-0		
KMRSTD4	55-6		
KXTLBA	53-6		
KMCD04	54-3		
KMCZA04	54-3		
KMCZC04	54-3		
KMCZD0	54-3		

OUTPUTS	F/O-SH
KCSDFB	33-1
KMVEQA	33-0
KL600D4	37-1
	52-2
KL601D4	37-1
	52-2
KL602D4	37-1
	52-2
KL603D4	40-2
	52-2
KL604D4	37-1
	52-2
KL605D4	37-0
	52-2
KL607D4	37-1
	38-2
	52-2
KL608D4	37-1
	38-2
	52-2
KL609D4	37-1
	52-2
KLV1D0	34-2
	38-2



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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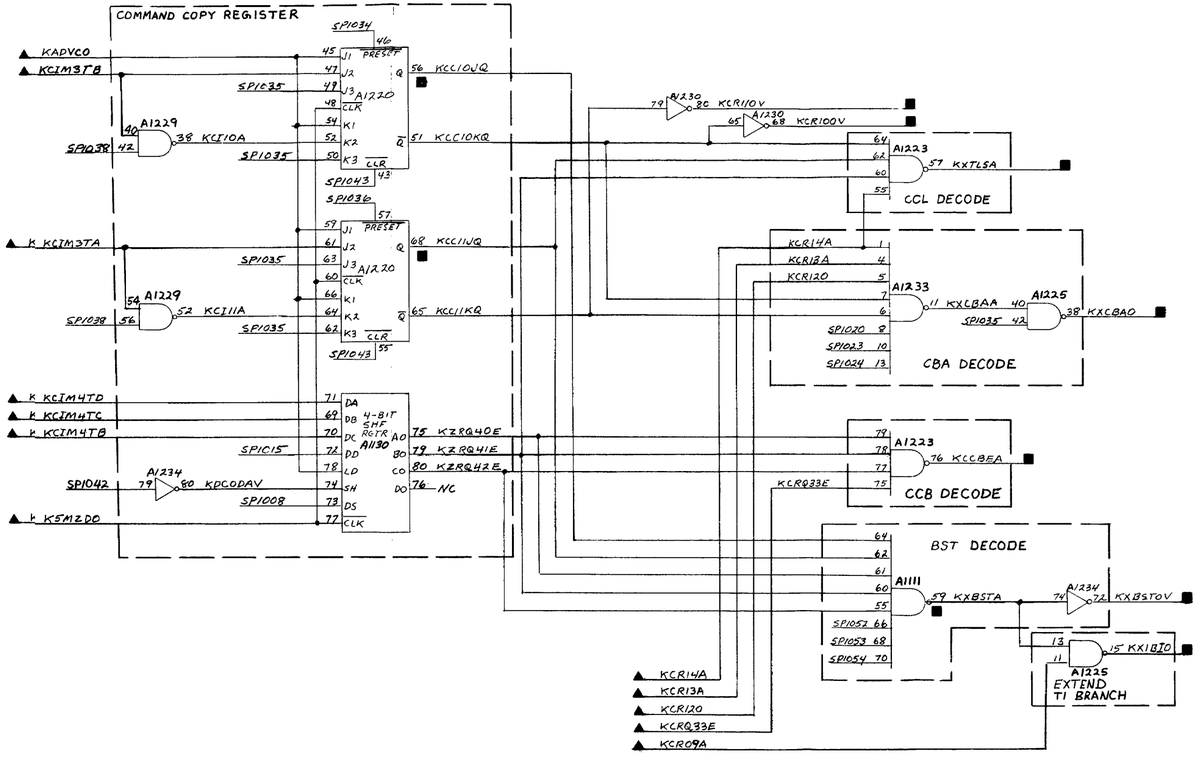
FO-22. Display Controller Low Speed Output Buffer Logic Diagram

INPUTS	F/O-SH
KADVC0	24-0
KCIM3TA	19-2
KCIM3TB	19-2
KCIM4TB	19-2
KCIM4TC	19-2
KCIM4TD	19-2
KCRQ33E	19-2
KCR09A	19-2
KCR13A	19-2
KCR14A	19-2
K5MZD0	54-3

OUTPUTS	F/O-SH
KCCBEA	27-0
KCC10JQ	26-1
KCC11JQ	26-1
KCR100V	18-2
KCR110V	18-2
KCR120	19-2
KXBSTA	17-1
	19-1
	27-0
KXBST0V	26-1
KXCBA0	16-1
KXTLSA	17-1
	20-0
	22-0
KX1BI0	17-1
	26-2



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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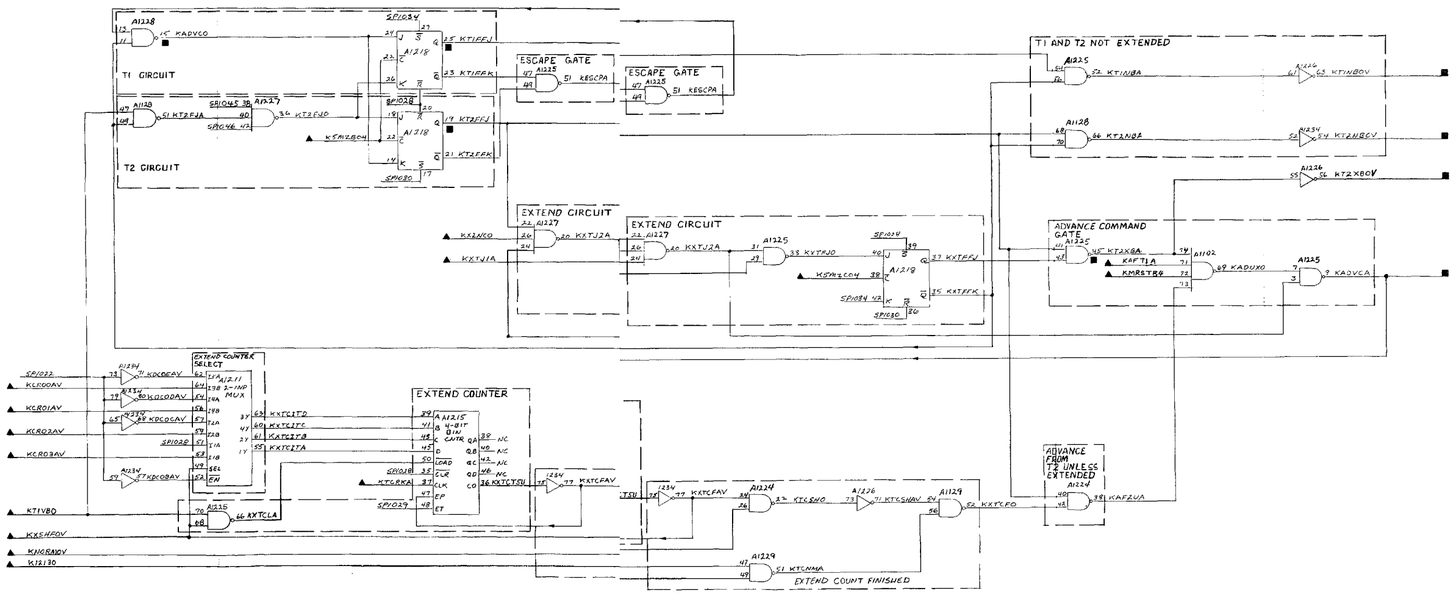
FO-23. Display Controller Timing and Control Command Copy Register Logic Diagram

INPUTS	F/O-SH	OUTPUTS	F/O-SH
KAFT1A	26-2	KADVCA	19-1
KCR00AV	19-2	KADVC0	19-2
KCR01AV	19-2		23-0
KCR02AV	19-2	KT1FFJ	26-1
KCR03AV	19-2	KT1NB0V	26-2
KMRSTB4	23-0		27-0
KN0RM0V	26-2	KT2FFJ	16-2
KT1VB0	26-2		16-4
KXSHF0V	26-1		26-2
KXTJ1A	26-2	T2NB0V	26-1
KXZNC0	26-2	KT2XB0A	27-0
K12130	16-4	KT2XB0V	26-1
K3MZB04	34-3		



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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FO-24. Display Controller Timing and Control Command Timing Logic Diagram

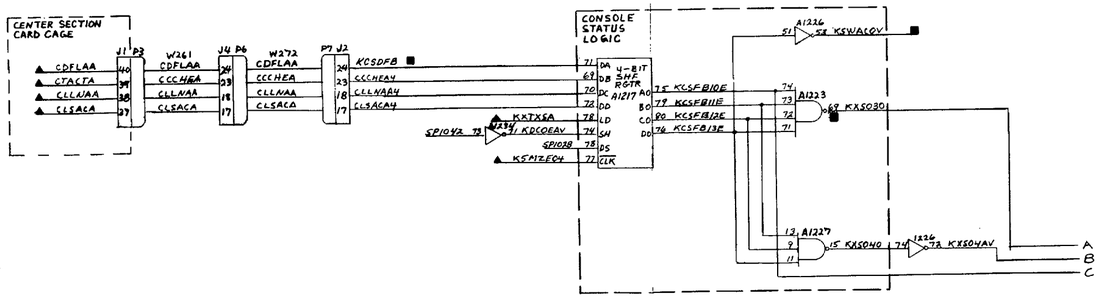
INPUTS	F/O-FIG	OUTPUTS	F/O-FIG
CDFLAA	40-2	KCSDFB	22-0
CLLNAA	37-3	KSLSTB4	36-1
CLSACA	37-1	(KSLSTB4)	
CTACTA	37-2	KSTPL0	26-1
KCR00AV	19-2	KSWAC0V	34-2
KCR01AV	19-2		36-2
KCR02AV	19-2		36-3
KCR03AV	19-2	KSW06D4	08-1
KCR04AV	19-2	KSW07D4	08-1
KCR05AV	19-2	KSW08D4	08-2
KCR06AV	19-2	KSW07D4	36-1
KCR07A	19-2	KXS030	26-2
KCR08A	19-2		
KCR09A	19-2		
KCR12A	19-2		
KDBRFJ	28-0		
KDBRR5V	26-1		
KDB043E	30-2		
KGRSWA	26-1		
KGSSWA	26-1		
KXTXSA	26-1		
K5MZBAH	54-3		
K5MZE04	54-3		
LDCRS0V	53-0		
VRRDY0	36-2		
VRSMP04	32-0		

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.



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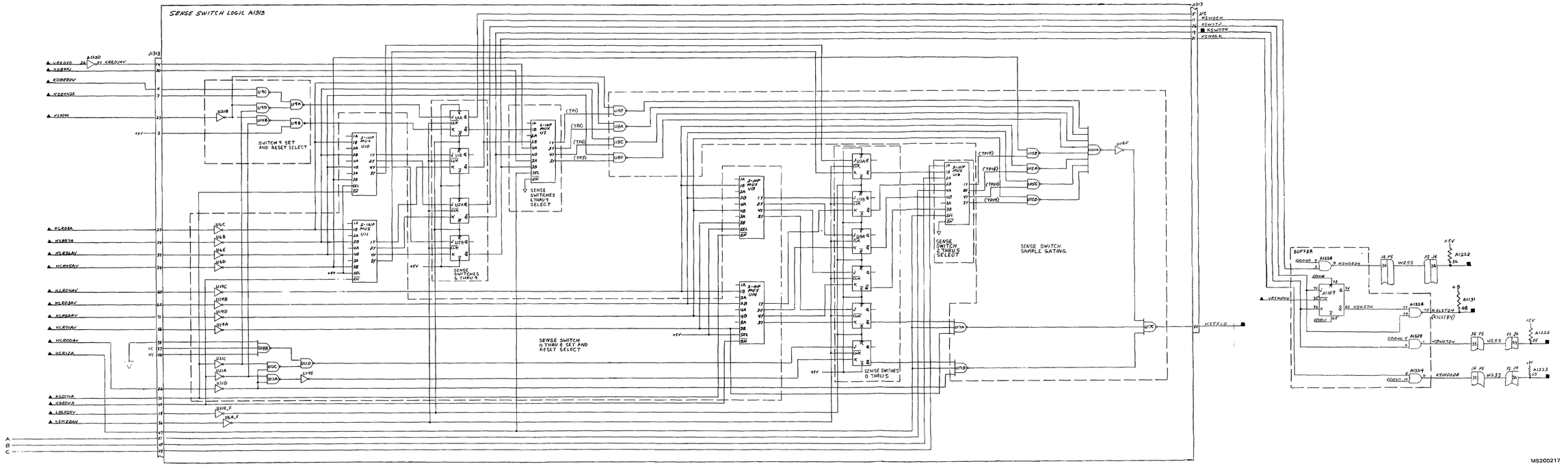
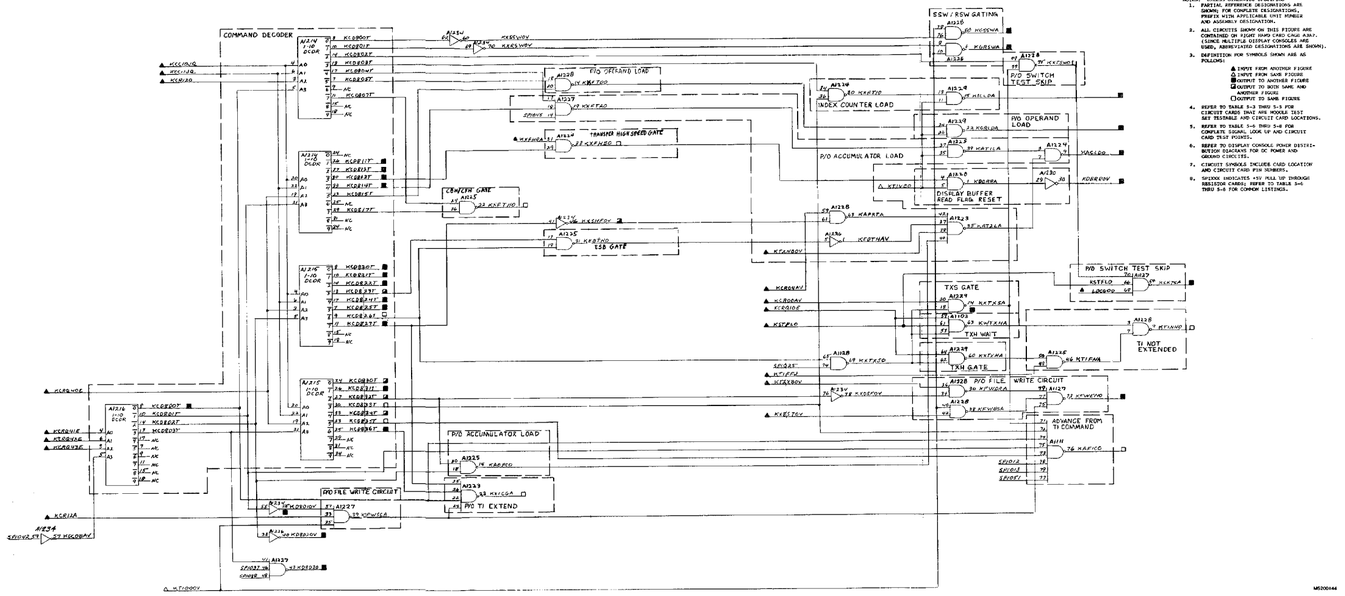
FO-25. Display Controller Timing and Control Sense Switch Logic Diagram (Sheet 1 of 2)



FO-25. Display Controller Timing and Control Sense Switch Logic Diagram (Sheet 2 of 2)



INPUTS	F/O-SH	INPUTS	F/O-SH	OUTPUTS	F/O-SH	OUTPUTS	F/O-SH
KAC12AV	16-2	KT2XBSV	24-5	KACL00	16-2	KD6D00	27-6
KA14SA	16-4	KT2XBSV	24-5		16-4	KFWKN0	17-3
KA09C0	16-4	KX3ET0V	23-5	KAF11A	24-2	KGRUWA	25-2
KCC14CQ	22-3	KXFTBFA	19-2	KCD00T	27-3	KGSUWA	25-2
KCC11CQ	22-3	KX1380	23-3	KCD01T	23-3	KRRLDA	29-5
KCD01T	16-1	KX0550	25-1	KCD02T	23-3	KSCE00	17-1
KCF6CFA	19-2	KXF12AV	16-3	KCD03T	23-5	KSCLDA	17-1
KCR6U0L	15-2	LDC000	45-8	KCD04T	16-1	KW6RM0V	24-6
KCR6U0E	15-2	YTEETR	25-5	KCD02MT	16-1	KR3EEA	52-1
KCR6U0E	15-5			KCD03TT	16-1	KRK3WA	19-1
KCR6U1L	19-2			KCD05TT	16-1	KSKEDA	19-1
KCR6U1E	19-2			KCC02ST	16-3	KRK3MCA	19-1
KCR6U1E	19-3			KCE02AT	16-1	KSKTEA	19-1
KCD06AV	19-2			KCU05T	16-3	KTIVB0	19-1
KCR06AV	19-2			KCD07T	16-1		24-1
KCR12A	19-2				27-1	KT0SF0	16-2
KCR120	19-2			KCD10ST	16-1	KKBTW0	27-5
KDB4CAV	28-0				17-2	KX0HF4V	16-2
KD88PK	28-2			KCD03T	19-1		16-4
KD0B3N	28-2			KCD05T	19-1		24-2
KDTYCA	17-1			KCD04T	19-1	KX7J1A	24-3
KLKBFK	32-2			KCD06T	19-1	KX7X8A	25-1
KRFFL6	25-2			KCR03N0	25-2	KX0NC0	24-2
KT1RFFJ	24-2				24-2	K0RLDA	16-2
KT1RD0V	24-2			KD6D0V	27-6		
KTEFF2	24-3			KD6D0V	27-2		

NOTES: UNLESS OTHERWISE SPECIFIED.
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATIONS, PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON EIGHT DMS 2740-2748 A30-1 (SLOWLY MULTIPLE DISPLAY CONTROLLER CARDS). REFER TO TABLE 3-4 FOR LOCATIONS.
3. DEFINITION FOR SYMBOLS SHOWN ARE AS FOLLOWS:
   - ▲ INPUT FROM ANOTHER FIGURE
   - △ INPUT FROM SAME FIGURE
   - ■ OUTPUT TO ANOTHER FIGURE
   - ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   - □ OUTPUT TO SAME FIGURE
4. REFER TO TABLE 3-3 THRU 3-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 3-6 THRU 3-8 FOR CIRCUIT CARDS THAT LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATION AND CIRCUIT CARD PIN NUMBERS.
8. SYGNAL INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 3-4 THRU 3-8 FOR COMMON LISTINGS.

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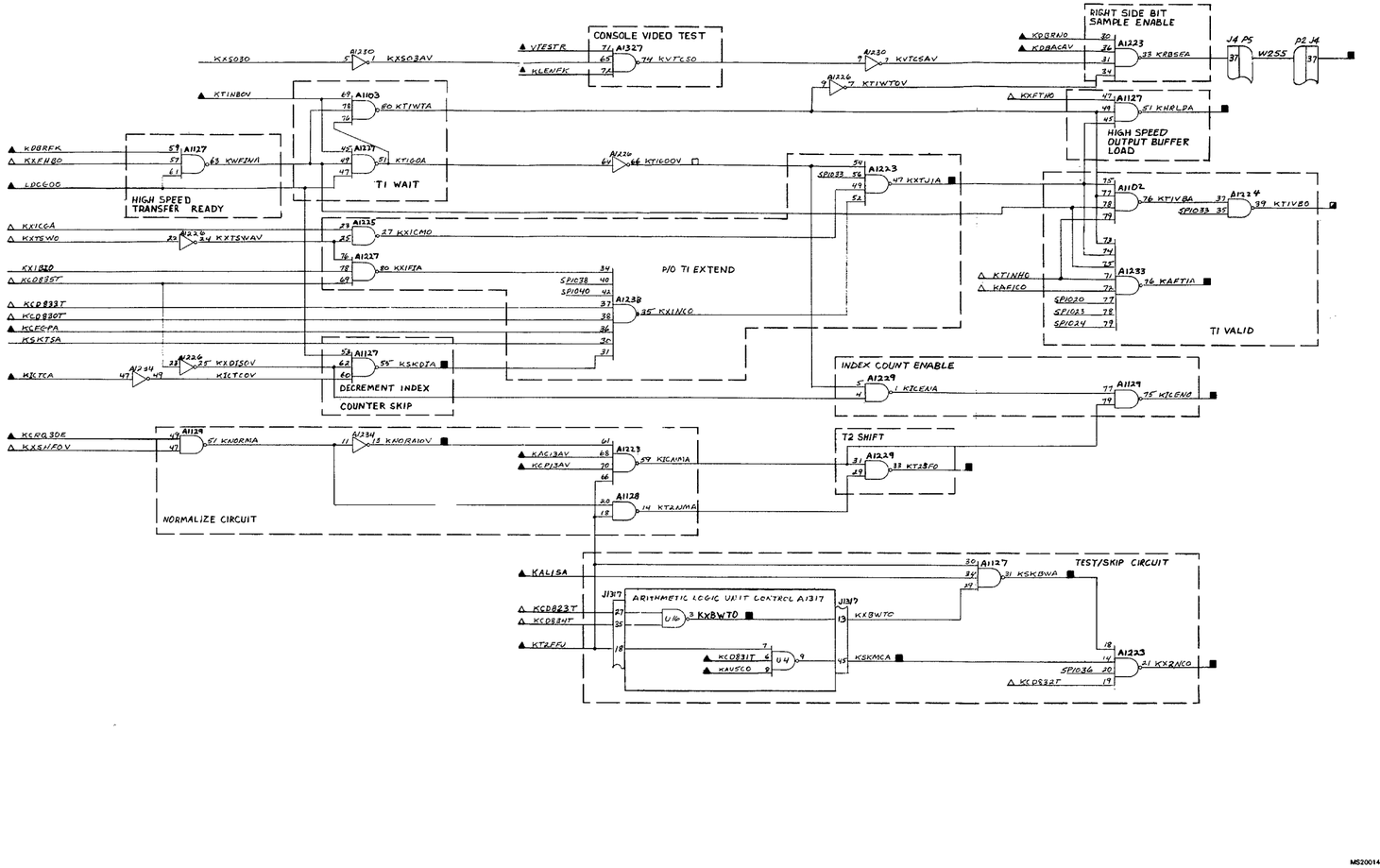
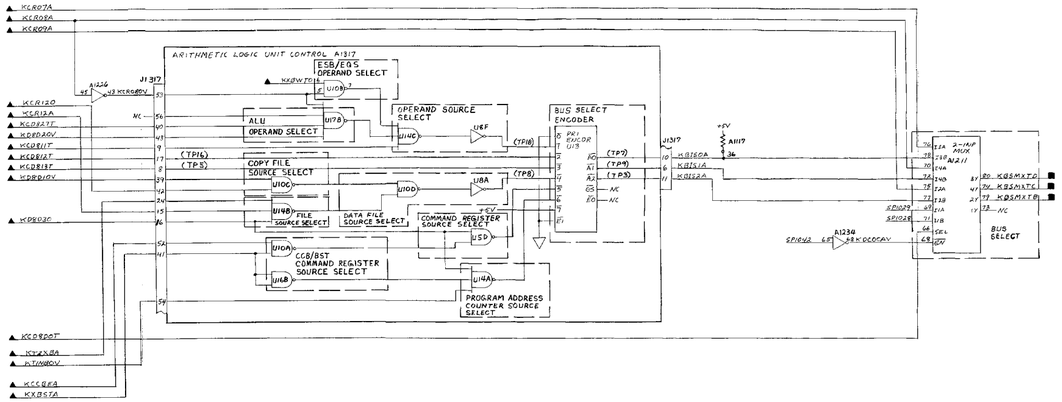
FO-26. Display Controller timing and Control Instruction decode logic diagram (Sheet 1 of 2)



FO-26. Display Controller Timing and Control Instruction Decode Logic Diagram (Sheet 2 of 2)

INPUTS	F/O-SH	OUTPUTS	F/O-SH
KCCBEA	23-0	KBSMXTB	18-1
KCD8D0T	26-1		52-3
KCD811T	26-1	KBSMXTC	18-1
KCD81ET	26-1		52-3
KCD812T	26-1	KBSMXTD	18-1
KCD82TT	26-1		52-3
KCR07A	19-2		
KCR08A	19-2		
KCR09A	19-2		
KCR12A	19-2		
KCR15S	19-2		
KDSD10V	26-1		
KDSD20V	26-1		
KDSD30	26-1		
KTINB0V	24-0		
KTZXBA	24-0		
KXBSTA	23-0		



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATIONS, PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON RIGHT HAND CARD CAGE A3A2. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITION FOR SYMBOLS SHOWN ARE AS FOLLOWS:
   - ▲ INPUT FROM ANOTHER FIGURE
   - △ INPUT FROM SAME FIGURE
   - ■ OUTPUT TO ANOTHER FIGURE
   - ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   - □ OUTPUT TO SAME FIGURE
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATION AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTINGS.

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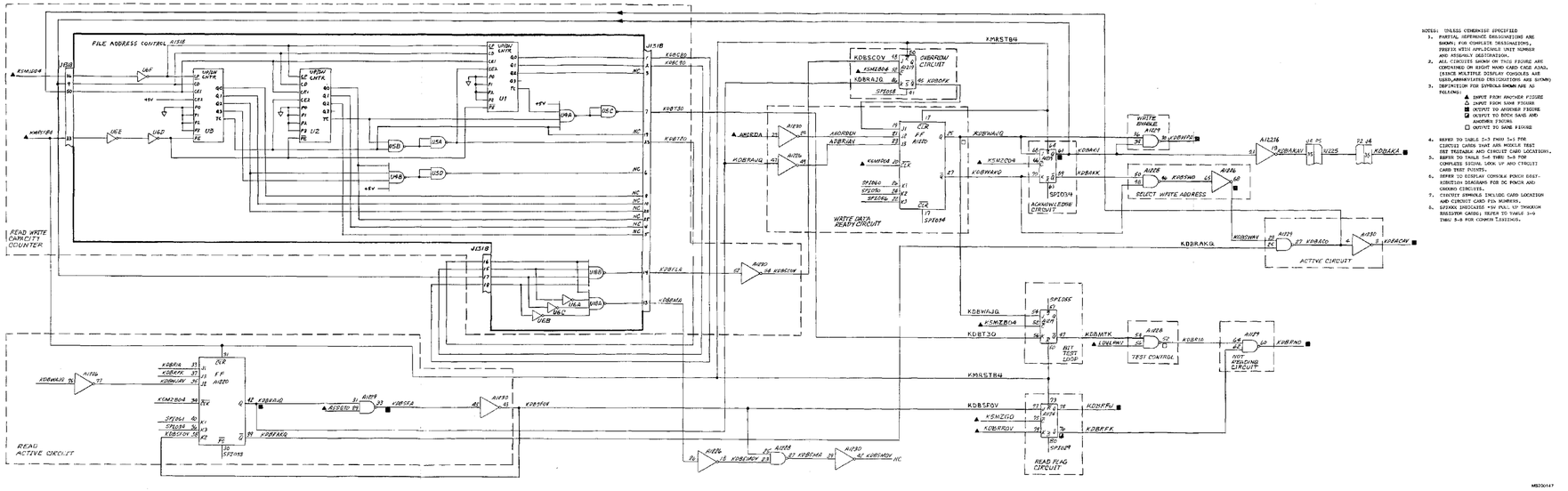
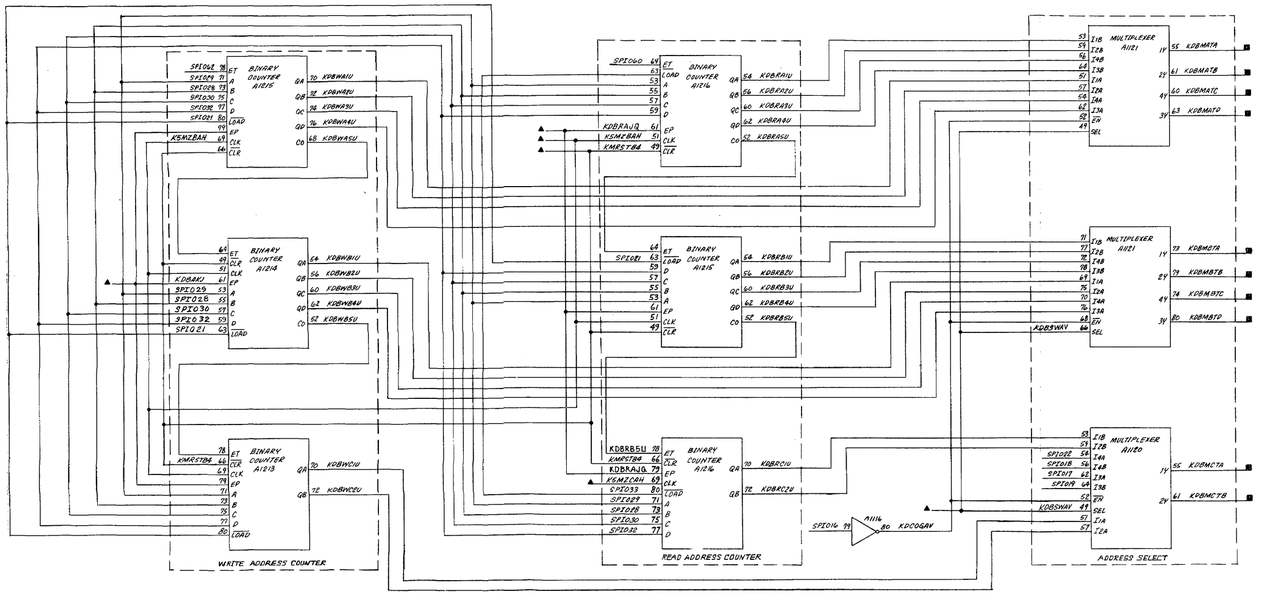
FO-27. Display Controller Timing and Control Data Bus Select Logic Diagram



INPUTS	F/O - SP	OUTPUTS	F/O - SP
A0ARDA	10-0	KDBACAV	25-2
A1AQTT	54-3	KDBAKA	10-0
KDBRIBV	26-1	KDBAKJ	29-0
KMRST84	63-0	KDBHAFQ	29-0
KSMZE04	54-2	KDBSFZ	25-2
KSMZC04	54-3	KDBBFK	26-2
KSMZC0	54-3	KDBRNB	26-2
KSMZD04	54-3	KDBSFA	30-2
LDVLPAV	49-0	KDBWAV	23-0
		KDBWPA	33-2

FO-28. Display Buffer Control Logic Diagram

INPUTS	F/O - SH	OUTPUTS	F/O - SH
KDBAKJ	28-6	KDBMATA	30-2
KDBRAJQ	28-6	KDBMATB	30-2
KDBSWAV	28-6	KDBMATC	30-1
KMRSTB4	53-6	KDBMATD	30-1
KSMZBAH	54-3	KDBMBTA	30-2
KSMZCAH	54-3	KDBMBTB	30-2
		KDBMBTC	30-2
		KDBMBTD	30-2
		KDBMCTA	30-2
		KDBMCTB	30-2



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS, PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON RIGHT HAND CARD CAGE A1A2, (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITION FOR SYMBOLS SHOWN ARE AS FOLLOWS:
   - ▲ INPUT FROM ANOTHER FIGURE
   - △ INPUT FROM SAME FIGURE
   - ● OUTPUT TO ANOTHER FIGURE
   - ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   - □ OUTPUT TO SAME FIGURE
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATION AND CIRCUIT CARD PIN NUMBERS.
8. SP100X INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTINGS.

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FO-29. Display Buffer Read/Write Address Counter Logic Diagram

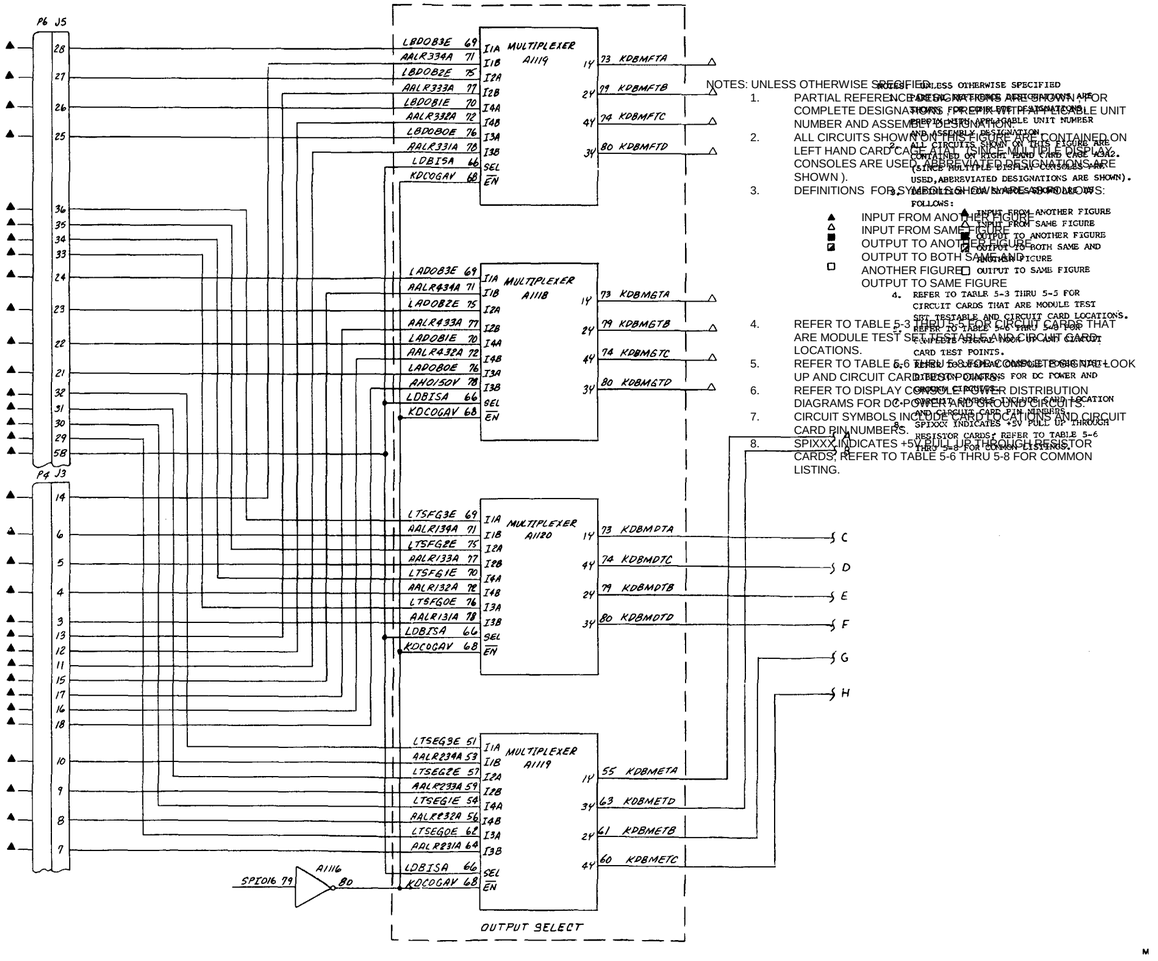
INPUTS	F/O - SH
AALR131A	10-0
AALR132A	10-0
AALR133A	10-0
AALR134A	10-0
AALR231A	10-0
AALR232A	10-0
AALR233A	10-0
AALR234A	10-0
AALR331A	10-0
AALR332A	10-0
AALR333A	10-0
AALR334A	10-0
AALR432A	10-0
AALR433A	10-0
AALR434A	10-0
AH0150V	10-0
KDBMATA	29-0
KDBMATB	29-0
KDBMATC	29-0
KDBMATD	29-0
KDBMBTA	29-0
KDBMBTB	29-0

INPUTS	F/O - SH
KDBMBTC	29-0
KDBMBTD	29-0
KDBMCTA	29-0
KDBMCTB	29-0
KDBSFA	28-0
KDBWPA	28-0
KSMZCAH	54-3
LAD0B0E	48-1
LAD0B1E	48-1
LAD0B2E	48-1
LAD0B3E	48-1
LBD0B0E	48-1
LBD0B1E	48-1
LBD0B2E	48-1
LBD0B3E	48-1
LDBISA	49-0
LTSEG0E	48-1
LTSEG1E	48-1
LTSEG2E	48-1
LTSEG3E	48-1

INPUTS	F/O - SH
LTSFG0E	48-1
LTSFG1E	48-1
LTSFG2E	48-1
LTSFG3E	48-1

OUTPUTS	F/O - SH
KDB010E	18-1
	52-2
KDB011E	18-1
	52-2
KDB012E	18-1
	52-2
KDB013E	18-1
	52-2
KDB020E	18-2
	52-2
KDB021E	18-2
	52-2
KDB022E	18-2
	52-2
KDB023E	18-2
	52-2
KDB030E	18-2
	52-2

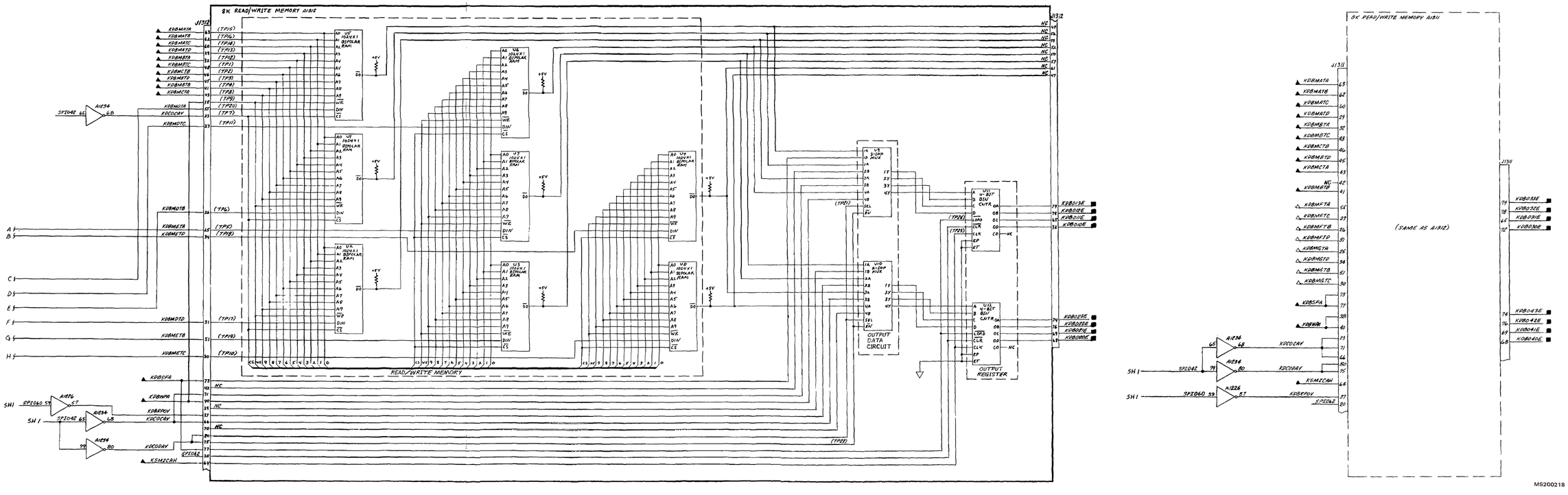
OUTPUTS	F/O - SH
KDB031E	18-2
	52-2
KDB032E	18-2
	52-2
KDB033E	18-2
	52-2
KDB040E	18-2
	52-2
KDB041E	18-2
	52-2
KDB042E	18-2
	52-2
KDB043E	25-2
	52-2



NOTES: UNLESS OTHERWISE SPECIFIED

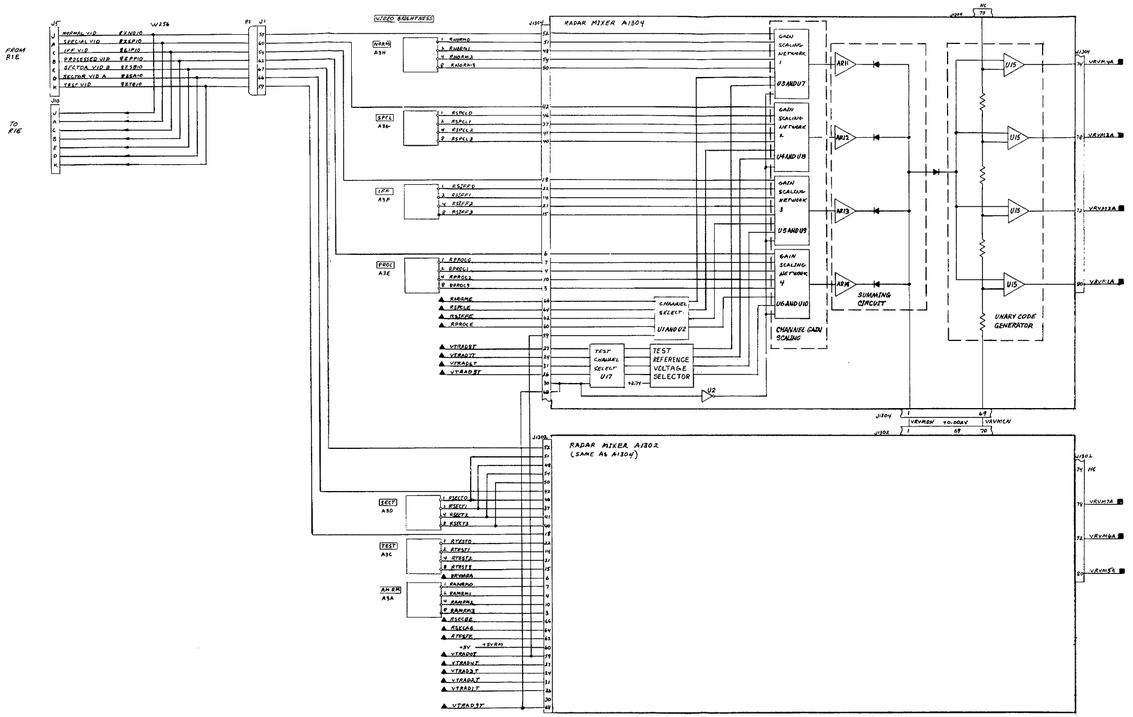
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN; FOR COMPLETE DESIGNATIONS PREFIX WITH ASSEMBLY OR CHASSIS NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE (SINCE ALL THREE CAGE WAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. SYMBOLOGY AND ABBREVIATIONS:
   - ▲ INPUT FROM ANOTHER FIGURE
   - △ INPUT FROM SAME FIGURE
   - ■ OUTPUT TO ANOTHER FIGURE
   - ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   - □ OUTPUT TO SAME FIGURE
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR DC COMPLETE TEST POINTS AND LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH A 2.2K RESISTOR CARDS, REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

FO-30. Display Buffer Read/Write Memory and Output Register Logic Diagram (Sheet 1 of 2)



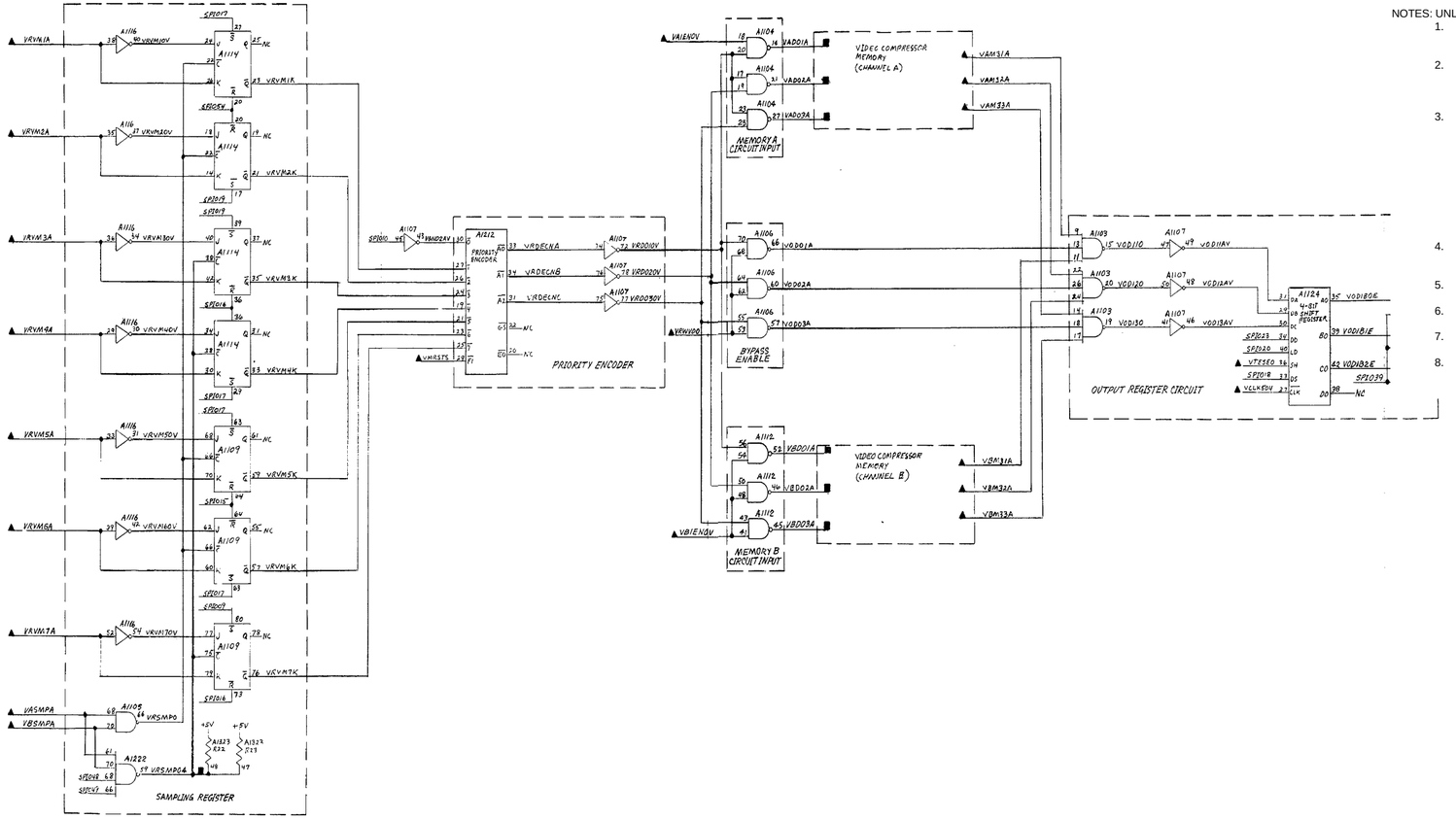
FO-30. Display Buffer Read/Write Memory and Output Register Logic Diagram (Sheet 2 of 2)

INPUTS	P/O – H1	OUTPUTS	P/O – H1
RNOEME	41-1	VRVM1A	32-0
RPBOCE	41-1		36-0
RHCCAE	41-1	VRVM2A	32-0
RHCCBE	41-1		36-0
RHFFE	41-1	VRVM3A	32-0
REPCLE	41-1		36-0
RTEFFE	41-1	VRVM4A	32-0
VRVMRA	34-1		36-0
VTRADNT	35-0	VRVM5A	32-0
VTRADIT	35-0		36-0
VTRADIT	35-0	VRVM6A	32-0
VTRADNT	35-0		36-0
VTRADET	35-0	VRVM7A	32-0
VTRADET	35-0		36-0
VTRADIT	35-0		
VTRADNT	35-0		
VTRADNT	35-0		
VTRADIT	35-0		


RADAR MIXER A1304
RADAR MIXER A1302
(SAME AS A1304)
FROM R1E
TO R1E
GAIN SCALING NETWORK I
GAIN SCALING NETWORK L
GAIN SCALING NETWORK S
GAIN SCALING NETWORK V
USANDUT
USANDUS
USANDUL
USANDUV
CHANNEL GAIN SCALING
SUMMING CIRCUIT
UNARY CODE GENERATOR
TEST CHANNEL SELECT U17
TEST REFERENCE VOLTAGE SELECTOR
CHANNEL SELECT
+6.2V
VRVM1A
VRVM2A
VRVM3A
VRVM4A
VRVM5A
VRVM6A
VRVM7A
VTRADNT
VTRADIT
VTRADET
VTRADIT
VTRADNT
VTRADET
VTRADIT
VTRADNT
VTRADET
VTRADIT
VTRADET
VTRADIT
VTRADET
+5V +5VRM
RHCCAE
RHCCBE
RHFFE
REPCLE
RTEFFE
RNOEME
RPBOCE
RNOEME
RPBOCE
RHCCAE
RHCCBE
RHFFE
REPCLE
RTEFF

INPUTS	F/O - SH
VA1EN0V	36-2
VAM31A	33-2
VAM32A	33-2
VAM33A	33-2
VASMPA	36-3
VB1EN0V	36-3
VBM31A	33-3
VBM32A	33-3
VBM33A	33-3
VBSMPA	36-3
VCLK504	54-3
VMRST5	36-1
VRVM1A	31-0
VRVM2A	31-0
VRVM3A	31-0
VRVM4A	31-0
VRVM5A	31-0
VRVM6A	31-0
VRVM7A	31-0
VRWVD0	34-1
VTES60	35-0

OUTPUTS	F/O - SH
VAD01A	33-1
VAD02A	33-1
VAD03A	33-1
VBD01A	33-2
VBD02A	33-2
VBD03A	33-2
V0D21D4	33-2
(V0D210L)	
V0D22D4	33-2
(V0D220L)	
V0D23D4	33-2
(V0D230L)	
VRSMP04	25-2



NOTES: UNLESS OTHERWISE SPECIFIED

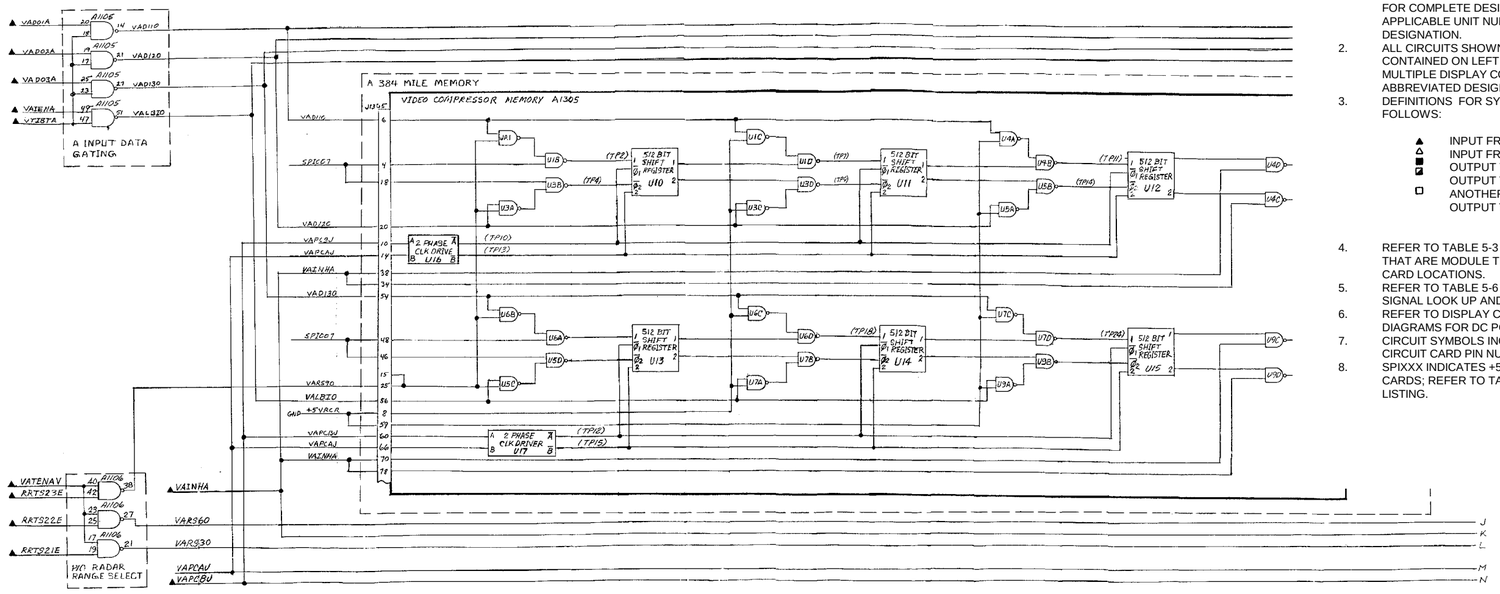
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING

FO-32. Video Compressor Input/Output Logic Diagram

INPUTS	F/O - SH	OUTPUTS	F/O - SH
RRTS21E	36-1	VAM11A	35-0
RRTS22E	36-1	VAM12A	35-0
RRTS23E	36-1	VAM13A	35-0
VAD01A	32-0	VAM14A	35-0
VAD02A	32-0	VAM21A	35-0
VAD03A	32-0	VAM22A	35-0
VAIENA	36-2	VAM23A	35-0
VAINHA	35-0	VAM24A	35-0
VAIEN0	36-2	VAM31A	32-0
VAPCAJ	36-5		35-0
VAPCBJ	36-6	VAM32A	32-0
VATENEV	35-0		35-0
VBD01A	32-0	VAM33A	32-0
VBD02A	32-0		35-0
VBD03A	32-0	VAM34A	35-0
VBIENA	36-3		36-2
VBINHA	35-0	VBM11A	35-0
VBIEN0	36-3	VBM12A	35-0
VBPCAJ	36-3	VBM13A	35-0
VBPCBJ	36-3	VBM14A	35-0
VBTENEV	35-0	VBM21A	35-0
VTIBTA	35-0	VBM22A	35-0
		VBM23A	35-0
		VBM24A	35-0
		VBM31A	32-0
			35-0
		VBM32A	32-0
			35-0
		VBM33A	32-0
			35-0
		VBM34A	35-0
			36-3



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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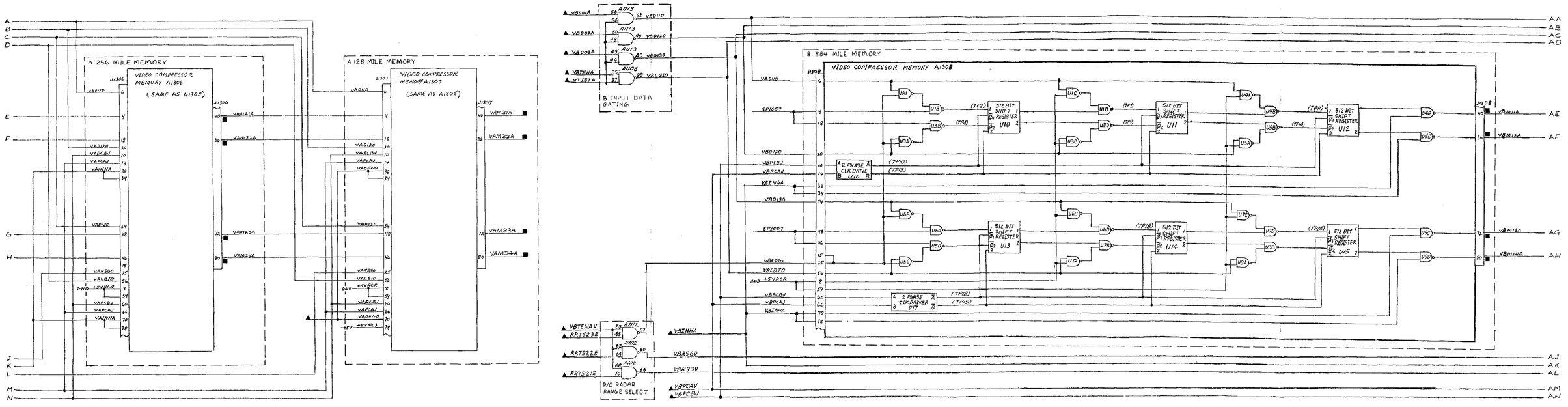
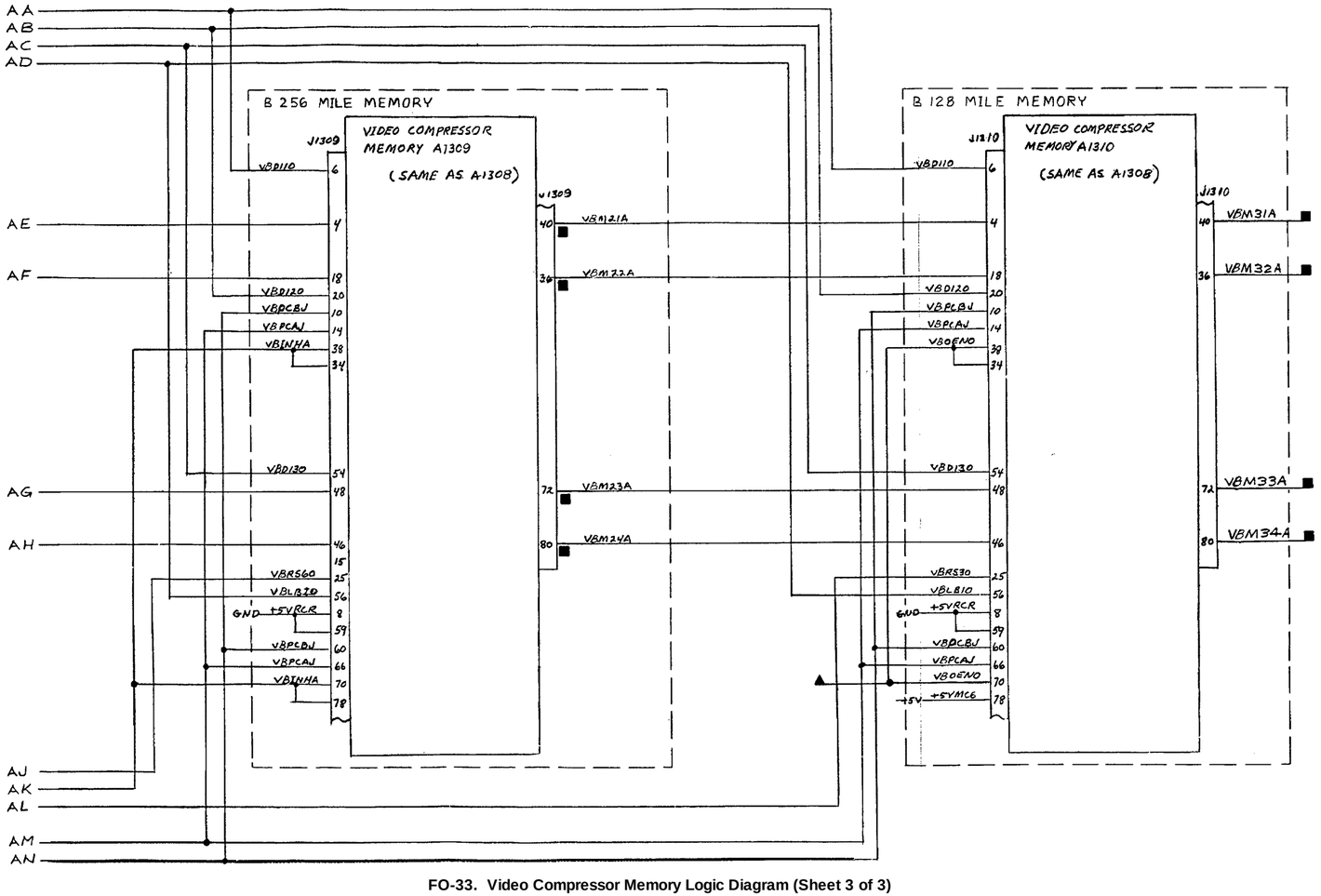
FO-33. Video Compressor Memory Logic Diagram
(Sheet 1 of 3)

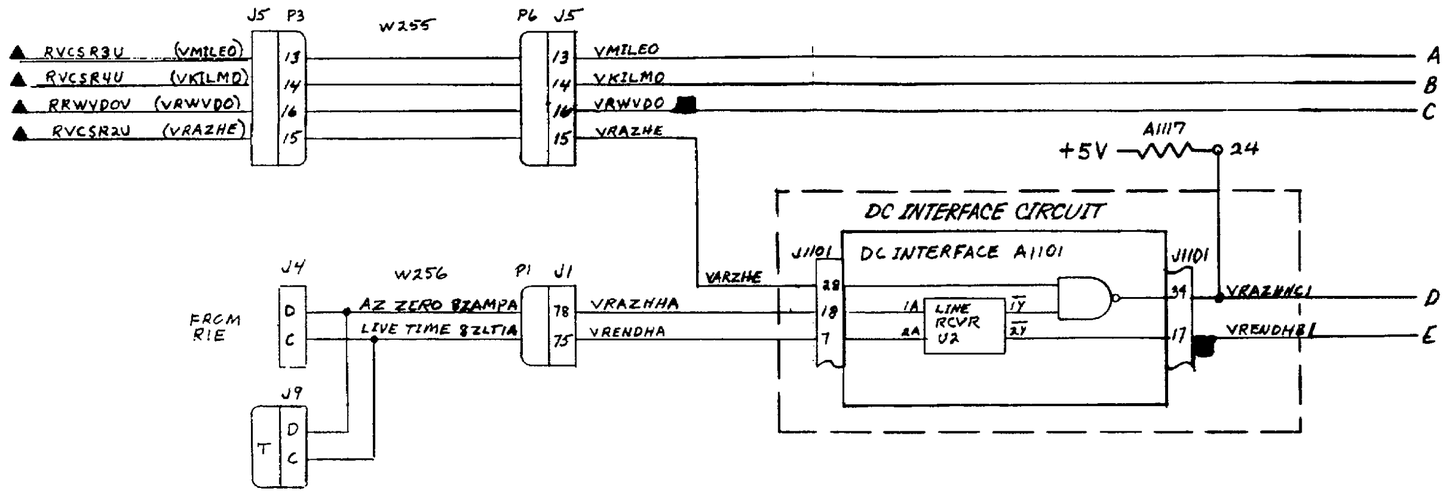


FO-33. Video Compressor Memory Logic Diagram (Sheet 2 of 3)



FO-33. Video Compressor Memory Logic Diagram (Sheet 3 of 3)

INPUTS	F/O - SH	OUTPUTS	F/O - SH
KSWAC0V	25-1	VRENDHB1	36-2
LVCTGD4	49-0		
RRWVDOV (VRWVDO)	41-4	VRENDHN4	36-2
RVCSR2U (VRAZHE)	41-4	VRLDEA	36-3 36-3
RVCSR3U (VMILEO)	41-4	VRLVT0	37-1
RVCSR4U (VKILMO)	41-4	VRMCA2U	35-0
VACLTA	36-2	VRMCA5U	35-0
VARMCA	36-3	VRMCB1U	35-0
VARMSA	36-3	VRVCB2U	35-0
VATENAV	35-0	VRMCB5U	35-0
VBCLTA	36-3	VRMC00	35-0
VBRMCA	36-3	VRMR2AV	35-0
VBRMSA	36-3	VRVMRA	31-0
VBTENAV	35-0	VRWVD0	22-0
VMRSBAV	36-1		32-0 36-1



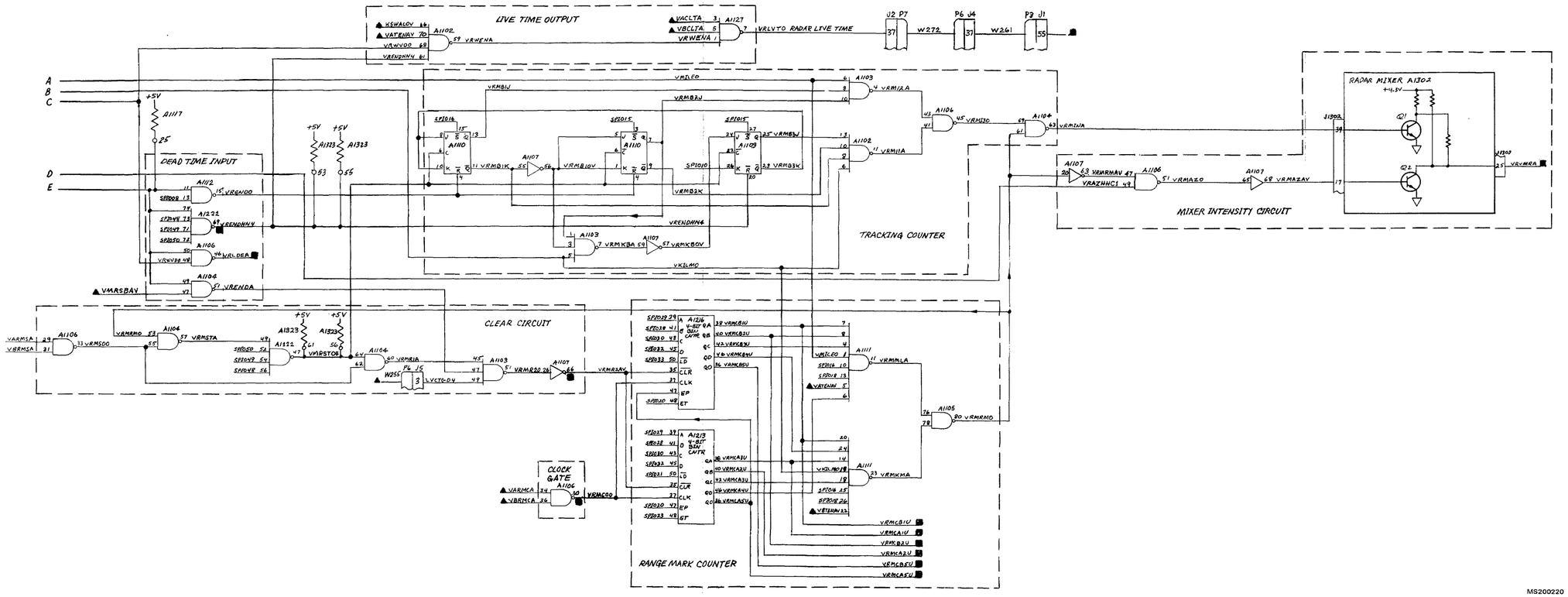
NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

FO-34. Video Compressor Range Mark and Azimuth Generator Logic Diagram (Sheet 1 of 2)



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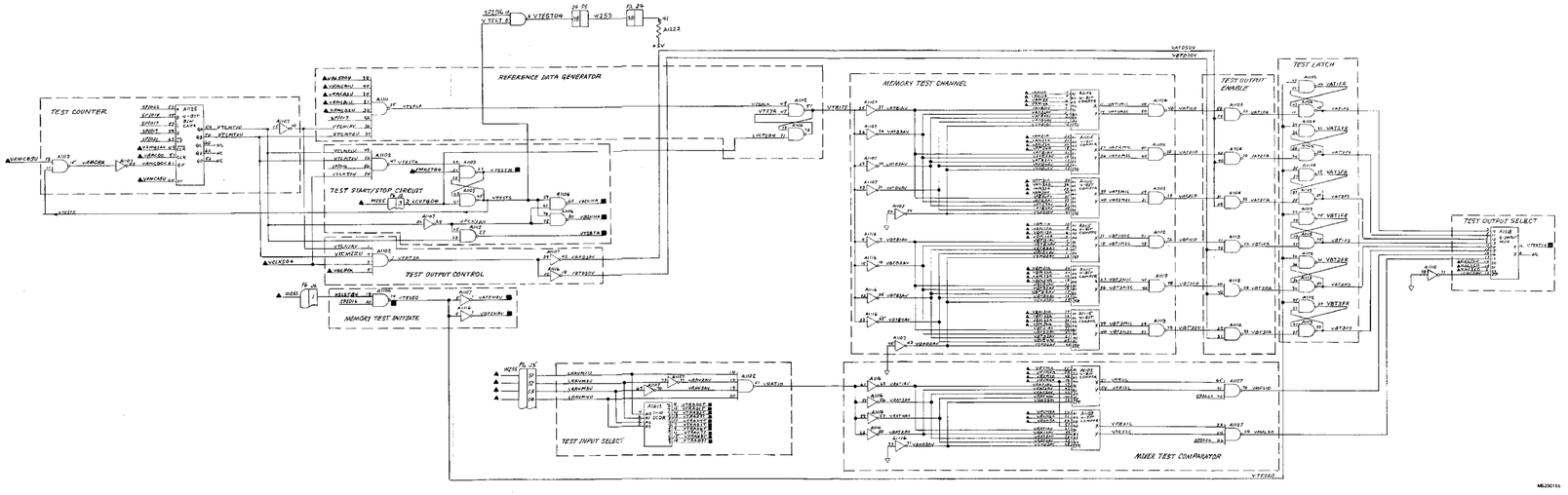
FO-34. Video Compressor Range Mark and Azimuth Generator Logic Diagram (Sheet 2 of 2)

INPUTS	F/O-SH	INPUTS	F/O-SH
KHC1C0	52-2	VBM13A	33-2
KHC2C0	52-2	VBM14A	33-2
KHC3C0	52-2	VBM21A	33-3
KMRSTB4	53-0	VBM22A	33-3
KSLSTB4	49-0	VBM23A	33-3
LCVTGD4	49-0	VBM24A	33-3
LRAVM1U	49-0	VBM31A	33-3
LRAVM2U	49-0	VBM32A	33-3
LRAVM3U	49-0	VBM33A	33-3
LRAVM4U	49-0	VBM34A	33-3
VACP1K	36-2	VCLK504	54-3
VAC50004	54-3	VRMCA1U	34-2
VAM11A	33-1	VRMCA2U	34-2
VAM12A	33-1	VRMCA5U	34-2
VAM13A	33-1	VRMCB1U	34-2
VAM 14A	33-1	VRMCB2U	34-2
VAM21A	33-1	VRMCB5U	34-2
VAM22A	33-2	VRMC00	34-2
VAM23A	33-2	VRMR2AV	34-2
VAM24A	33-2	VRVM1A	31-0
VAM31A	33-2	VRVM2A	31-0
VAM32A	33-2	VRVM3A	31-0
VAM33A	33-2	VRVM4A	31-0
VAM34A	33-2	VRVM5A	31-0
VBM11A	33-2	VRVM6A	31-0
VBM12A	33-2	VRVM7A	31-0

OUTPUTS	F/O-SH	OUTPUTS	F/O-SH
VAINHA	33-1	VTIBTA	33-1
VATENAV	33-1		33-2
	34-2	VTRAD0T	31-0
	36-2	VTRAD1T	31-0
VB1NHA	33-2	VTRAD2T	31-0
VBTENAV	33-2	VTRAD3T	31-0
	34-2	VTRAD4T	31-0
	36-3	VTRAD5T	31-0
VTESE0	32-0	VTRAD6T	31-0
VTESTR	26-2	VTRAD7T	31-0
	36-2	VTRAD8T	31-0
	36-3	VTRAD9T	31-0
VTEST1X	52-3		



FO-35. Video Compressor Test Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

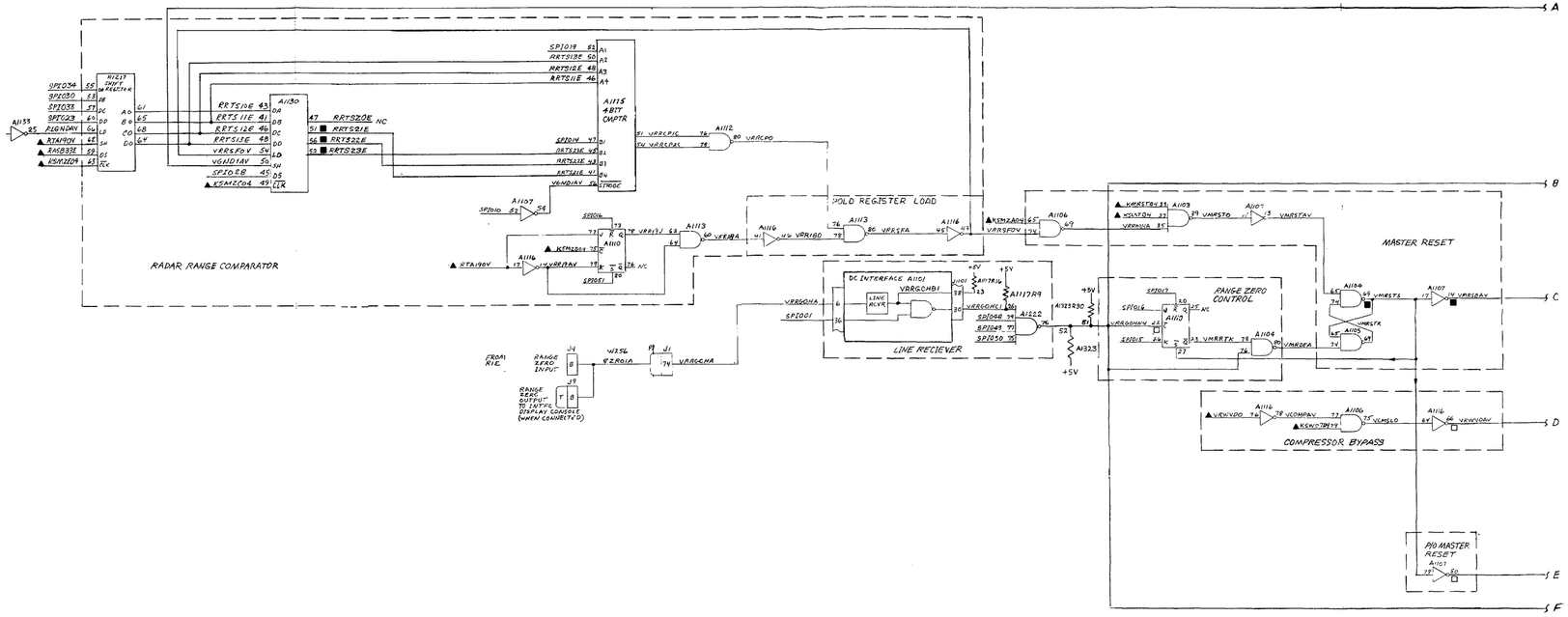
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

INPUTS	F/O- SH	INPUTS	F/O- SH
KMRSTB4	53-0	VATENAV	35-0
KSLSTB4	25-2	VBC5004	54-3
KSWAC0V	25-1	VBM34A	33-3
KSW07D4	25-2	VBGP60	54-3
KSMZA04	54_3	VBTENAV	35-0
KSMZB04	54-3	VCLK504	54-3
KSMZC04	54-3	VRENDHB1	34-1
KSMZE04	54-3	VRENDHN4	34-2
RASB33E	46-0	VRLDEA	34-2
RTA190V	41-2	VRWVD0	34-1
VACP60	54-3	VTESTR	35-0
VAC5004	54-3		
VAM34A	33-2		

OUTPUTS	F/O- SH	OUTPUTS	F/O- SH
RRTS21E	33-1	VARMSA	34-2
	33-2	VASMPA	32-0
RRTS22E	33-1	VBCENS	54-3
	33-2	VBCLTA	34-2
RRTS23E	33-1	VBIENA	33-2
	33-2	VBIENOV	32-0
VACENS	54-3	VB0EN0	33-3
VACLTA	34-2	VBPCAJ	33-2
VACP1K	35-0	VBPCBJ	33-2
VAIENA	33-1	VBRMCA	34-2
VAIEN0V	32-0	VBRMSA	34-2
VA0EN0	33-2	VBSMPA	32-0
VAPCAJ	33-1	VMRSBAV	34-2
VAPCBJ	33-1	VMRSTS	32-0
VARMCA	34-2	VRRDY0	25-2



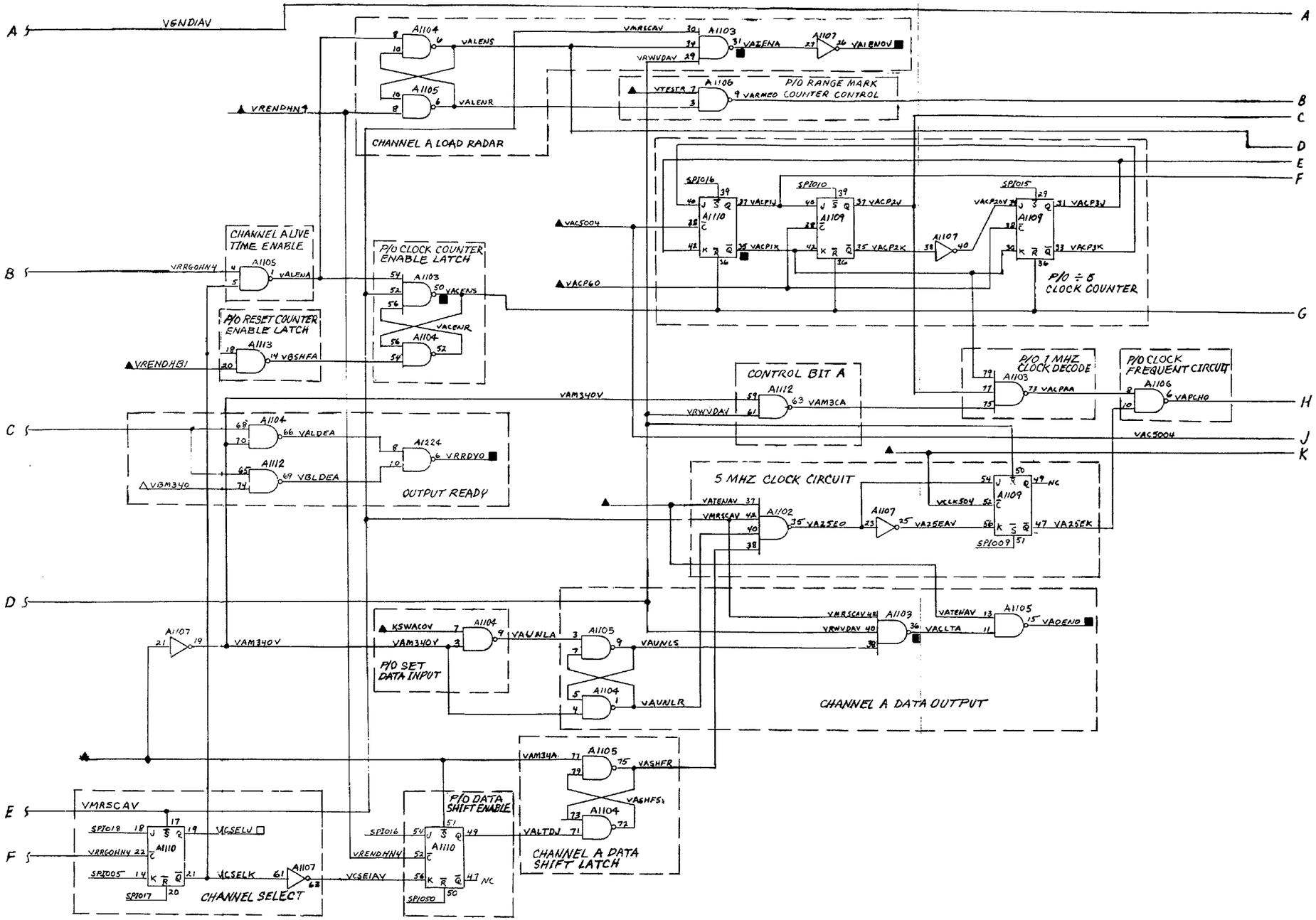
NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

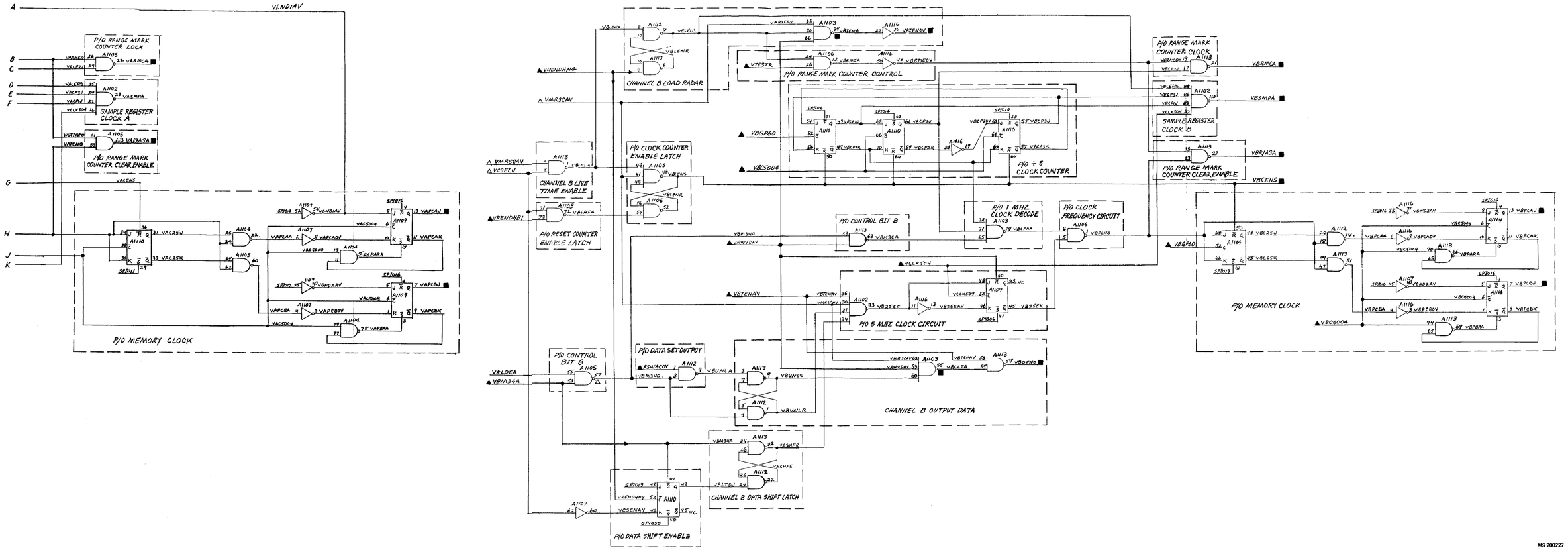
   ▲ INPUT FROM ANOTHER FIGURE
   Δ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ☑ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.

FO-36. Video Compressor Timing and Control Logic Diagram (Sheet 1 of 3)

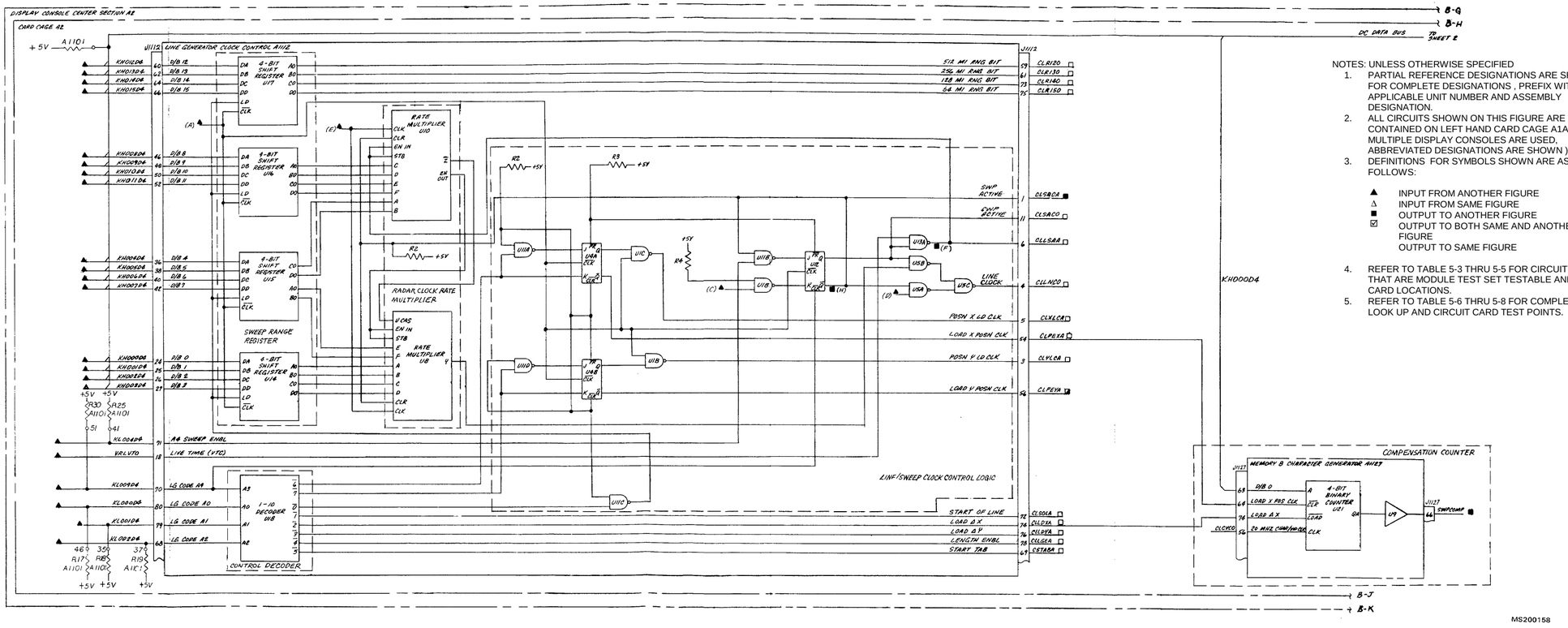


FO-36. Video Compressor Timing and Control Logic Diagram (Sheet 2 of 3)



FO-36. Video Compressor Timing and Control Logic Diagram (Sheet 3 of 3)

INPUTS	F/O-SH	OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
CCCHEA	38-2	CLDAXE	40-2	A1114(N)	52-8
CCRMCA	38-3	CLDAXW	40-2	A1114(P))	52-3
CLCVCO	54-1	CLDAYN	40-2	A1114(R)	52-4
CLDDCAS	54-1	CLDAYS	40-2	A1115(A))	52-4
KH000D4	20-0	CLLE4A	39-1	A1115(B))	52-4
KH001D4	20-0	CLLNAA	25-1	A1115(C))	52-4
KH002D4	20 0	CLPEYA	40-1	A1115(D)	52-4
KH003D4	20-0	CLOACA	25-1	A1115(E)	52-4
KH004D4	20-0	CLSVEA	39-2	A1115(F)	52-4
KH005D4	20-0	CLVDCO	39-2	A1115(G))	52-4
KH006D4	20-0	CLXDAT	52-4	A1115(H)	52-4
KH007D4	20-0	CLYDAT	52-4	A1115(I)	52-4
KH008D4	20-0	CSWLNA	54-1	A1115(J))	52-4
KH009D4	20-0	CTACTA	25-1	A1115(K))	52-4
KH010D4	20-0	SWPC0MP	39 2	A1115(L))	52-4
KH011D4	20-0	A1112(F))	54-1	A1115(M))	52-4
KH012D4	20-0	A1112(H))	54-1	A1115(N)	52-4
KH013D4	20-0	A1114(A)	52-4	A1115(P))	52-4
KH014D4	20-0	A1114(B)	52-4	A1115(R))	52-4
KH015D4	20-0	A1114(C))	52-4		
kl000D4	22-0	A1114(D)	52-4		
KLOOID4	21-0	A1114(E)	52-4		
KL002D4	22-0	A1114(F)	52-4		
KL004D4	22-0	A1114(G)	52-4		
KL009D4	22-0	A1114(H)	52-3		
VR1VT0	34-2	A1114(I)	52-3		
A1112(A)	64-1	A1114(J)	52-3		
A1112(C)	54-1	A1114(K)	52-3		
A1112(D)	54-1	A1114(4	52-3		
A1112(E))	54-1	A1114 (M)	52-3		



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   Δ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ☑ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.

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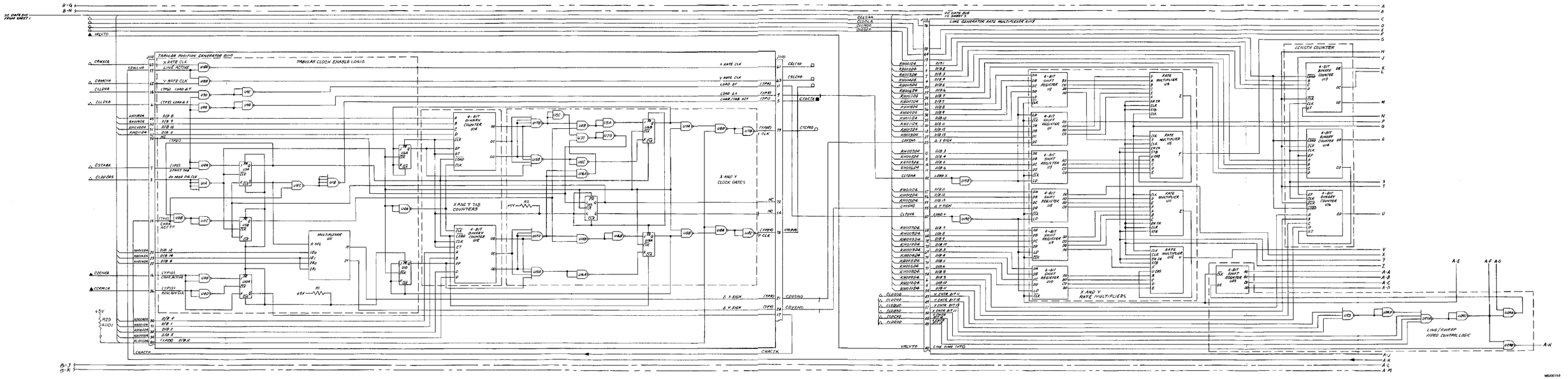
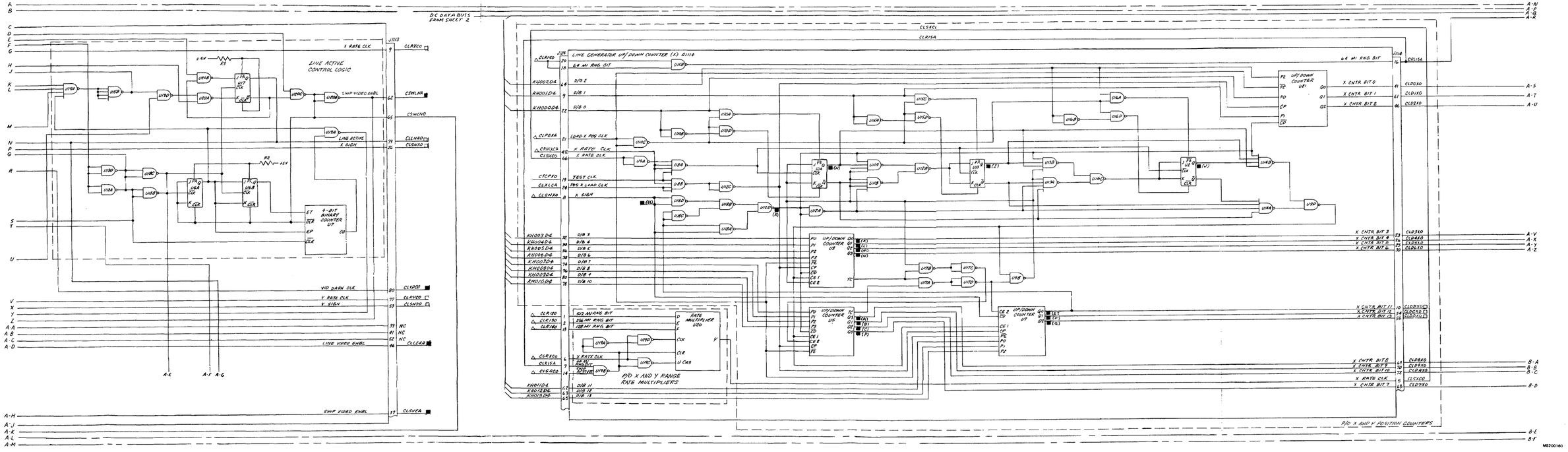
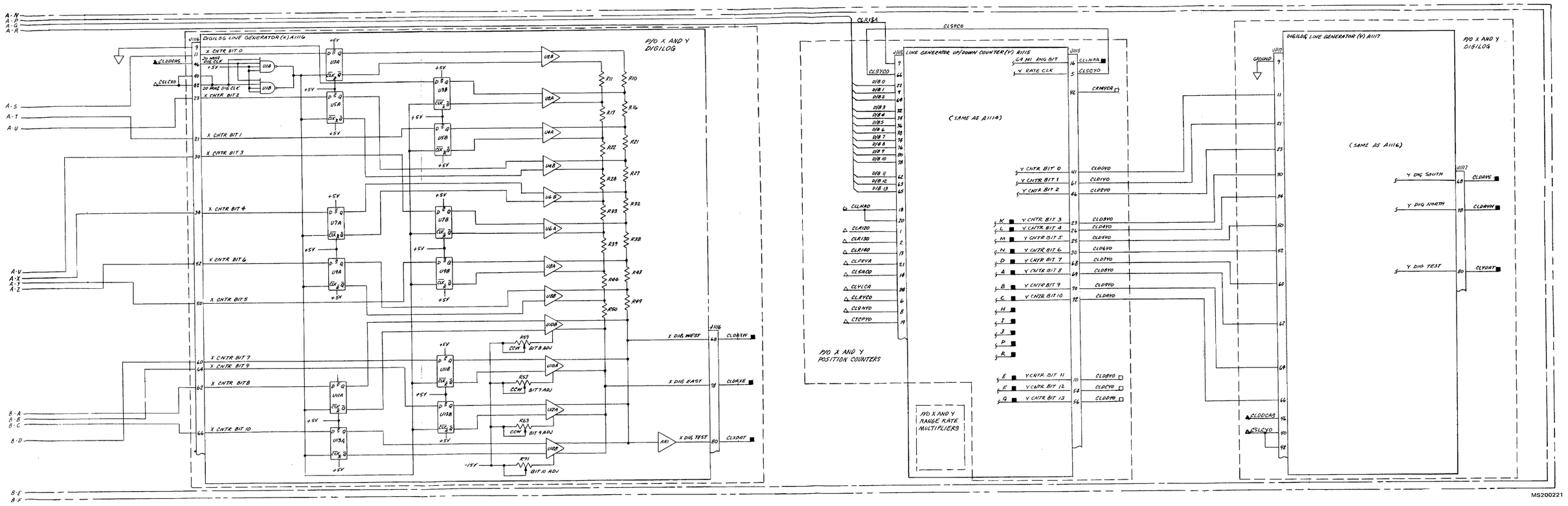
FO-37. Display Generator Line Generator Logic Diagram (Sheet 1 of 4)



FO-37. Display Generator Line Generator Logic Diagram (Sheet 2 of 4)



FO-37. Display Generator Line Logic Diagram (Sheet 3 of 4)



FO-37. Display Generator Line Logic Diagram (Sheet 4 of 4)

INPUTS	F/O - SH
CLCVC0	54-1
KH008D4	20-0
KH009D4	20-0
KH010D4	20-0
KH011D4	20-0
KH012D4	20-0
KH013D4	20-0
KH014D4	20-0
KL007D4	22-0
KL008D4	22-0

OUTPUTS	F/O - SH
CCCHEA	37-2
CCCVEA	39-2
CCDAXE	40-2
CCDAXW	40-2
CCDAYN	40-2
CCDAYS	40-2
CCRMCA	37-2
CCSTOA	52-3
CCXSN0	52-3
CCYSN0	52-3
A1126(A)	52-3
A1126(B)	52-4
A1126(C)	52-4
A1126(D)	52-4
A1126(E)	52-4
A1126(F)	52-4
A1126(G)	52-4
A1126(H)	52-4
A1126(I)	52-4
A1126(J)	52-4
A1126(K)	52-3
A1126(L)	52-3
A1126(M)	52-3

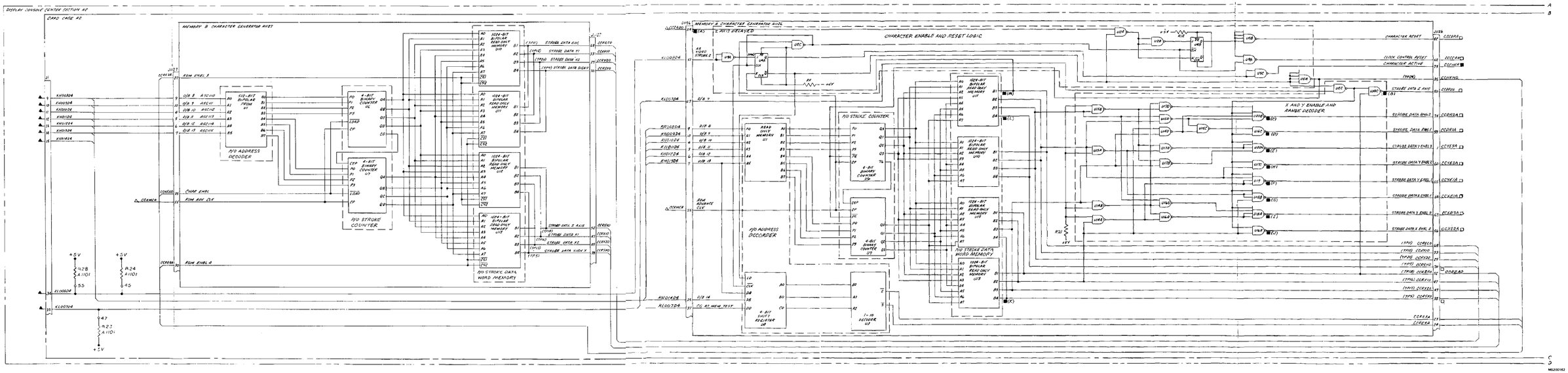
NOTES: UNLESS OTHERWISE SPECIFIED

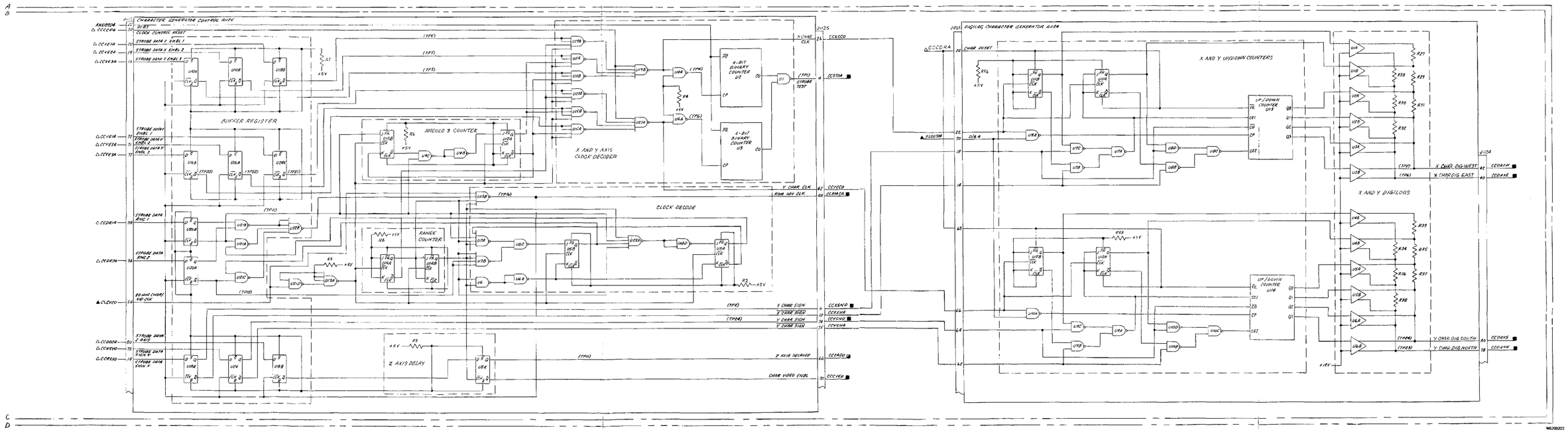
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.

FO-38. Display Generator Character Generator Logic Diagram (Sheet 1 of 3)


DISPLAY CONSOLE CENTER SECTION A2
CARD CAGE A2
MEMORY B CHARACTER GENERATOR A1A2
MEMORY A CHARACTER GENERATOR A1A2
CHARACTER ENABLE AND RESET LOGIC
X AND Y ENABLE AND RANGE DECODER
R/O ADDRESS DECODER
R/O STROBE COUNTER
R/O STROBE DATA WORD MEMORY
R/O ADDRESS DECODER
R/O STROBE COUNTER
R/O STROBE DATA WORD MEMORY
ROM ENABLE 3
ROM ENABLE 4
CHAR ENBL
ROM ADV CLK
ROM ADVANCE CLK
+5 AXIS DELAYED
CHARACTER RESET
CLOCK CONTROL RESET
CHARACTER ACTIVE
STROBE DATA Z ENBL
STROBE DATA X ENBL
STROBE DATA Y ENBL
STROBE DATA Z AXIS
STROBE DATA Y1
STROBE DATA Y2
STROBE DATA X1
STROBE DATA X2
STROBE DATA Y AXIS
STROBE DATA X AXIS
+5V
-10V
R27 A1101 47
R28 A1101 55
R24 A1101 45
R22 A1101 47
R21 A1101 47
R23 A1101 47
R25 A1101 47
R26 A1101 47
R29 A1101 47
R30 A1101 47
R31 A1101 47
R32 A1101 47
R33 A1101 47
R34 A1101 47
R35 A1101 47
R36 A1101 47
R37 A1101 47
R38 A1101 47
R39 A1101 47
R40 A1101 47
R41 A1101 47



FO-38. Display Generator Character Generator Logic Diagram (Sheet 3 of 3)

INPUTS	F/O - SH
CCCVEA	38-3
CLCVD0	54-1
CLLE4A	37-3
CLSVEA	37-3
CLVDC0	37-3
KH000D4	20-0
KH001D4	20-0
KH002D4	20-0
KH003D4	20-0
KH004D4	20-0
KH005D4	20-0
KH006D4	20-0
KH007D4	20-0
KH008D4	20-0
KH009D4	20-0
KH010D4	20-0
KH011D4	20-0
KH012D4	20-0
KH013D4	20-0
KH014D4	20-0
KH015D4	20-0
KLV1D0	22-0
SWPC0MP	37-1
V0D21 D4	32-0
V0D22 D4	32-0
V0D23 D4	32-0

OUTPUTS	F/O - SH
CVATBP	52-4

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
6. ▭ INDICATES FRONT PANEL MARKINGS.

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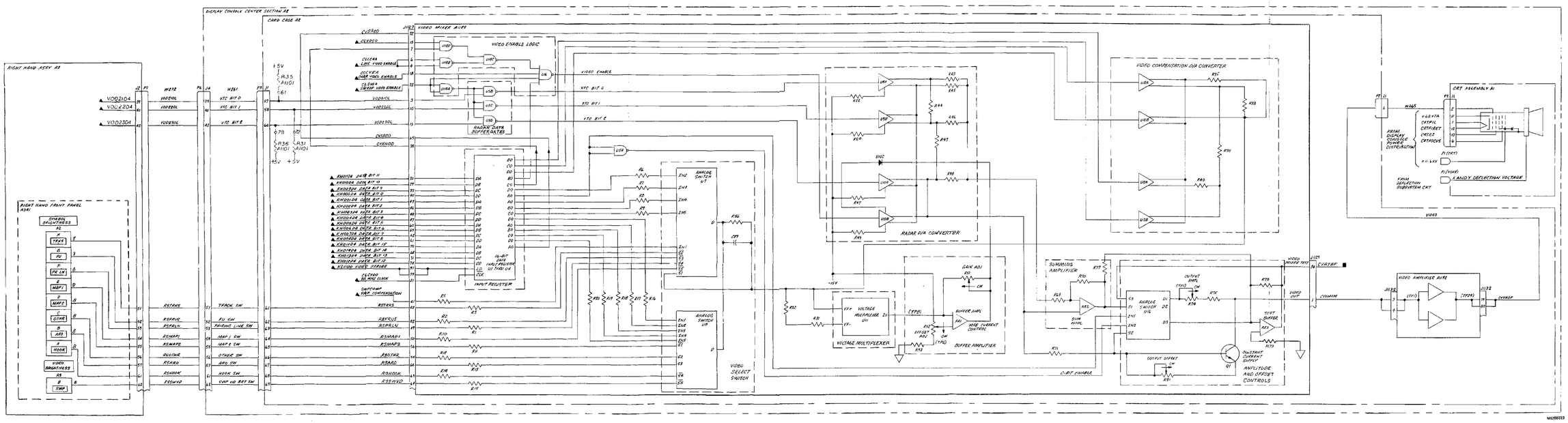
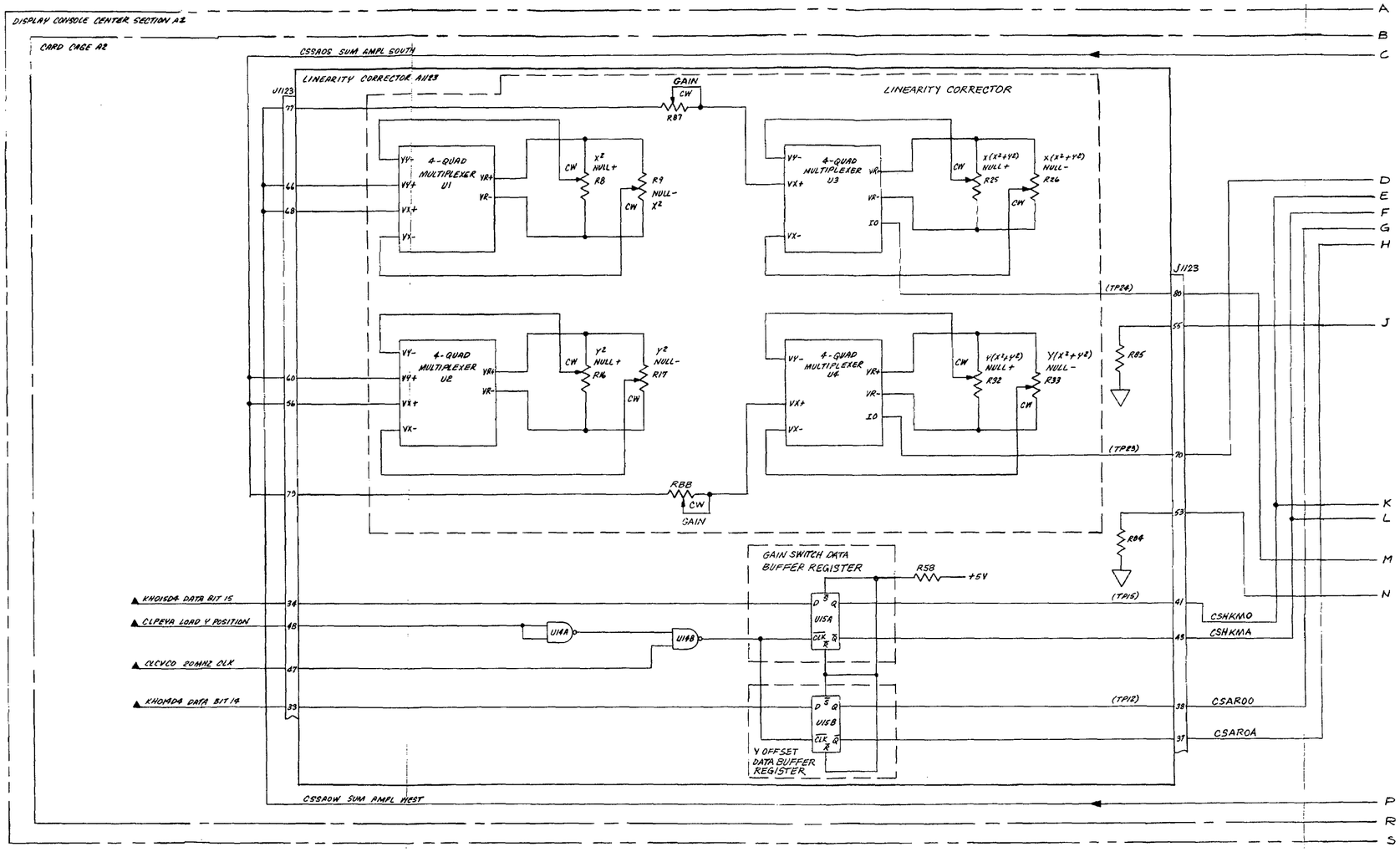
FO-39. Display Generator Video Subsystem Logic Diagram (Sheet 1 of 2)



FO-39. Display Generator Video Subsystem Logic Diagram
(Sheet 2 of 2)

INPUTS	F/O - SH	OUTPUTS	F/O - SH
CCDAXE	38-3	CDFLLA	25-1
CCDAXW	38-3	CDXTST	52-4
CCDAYN	38-3	CDYTST	52-4
CCDAYS	38-3	CSTBX0	52-4
CLCVC0	54-1	CSTBY0	52-4
CLDAXE	37-4		
CLDAXW	37-4		
CLDAYN	37-4		
CLDAYS	37-4		
CLPEYA	37-1		
KH015D4	20-0		
KH014D4	20-0		
KL003D4	22-0		



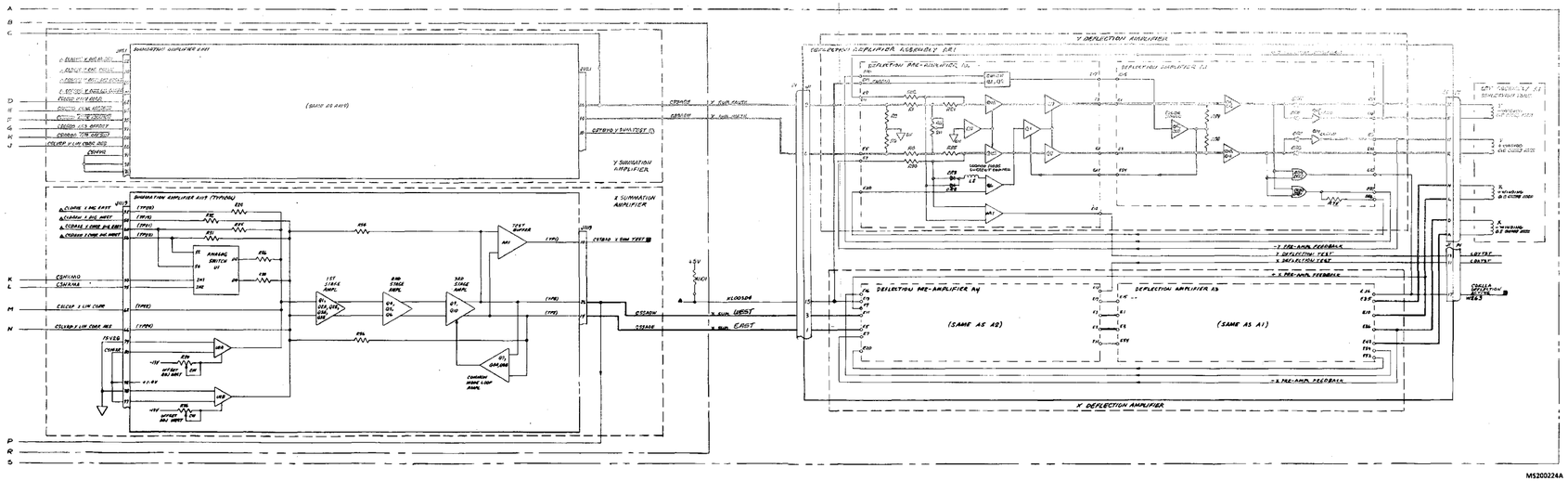
FO-40. Display Generator Deflection Subsystem Logic Diagram (Sheet 1 of 2)

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

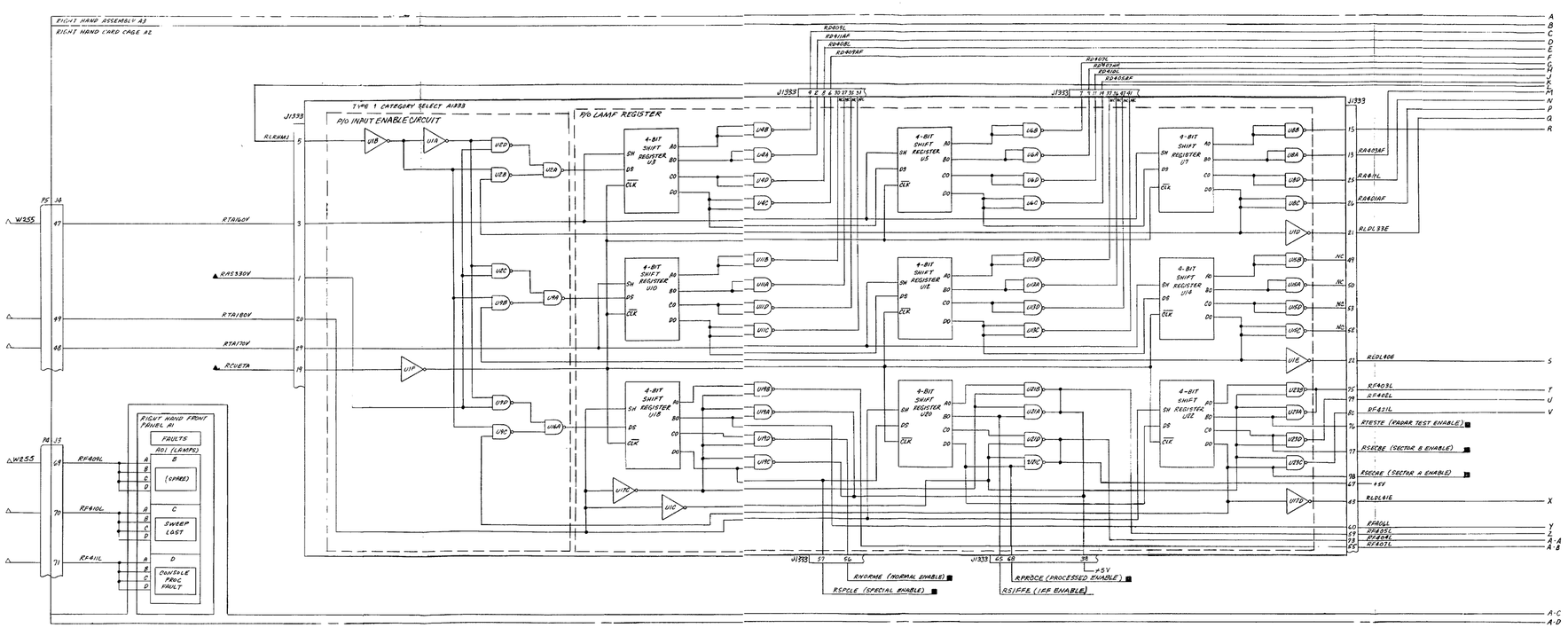
   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.



Change 1 FO-40. Display Generator Deflection Subsystem Logic Diagram (Sheet 2 of 2)

INPUTS	F/O - SH	OUTPUTS	F/O - SH
ALI11B	5-0	RNORME	31-0
ALI12B	5-0	ROACH0	43-0
ALI13B	5-0	RPROCE	31-0
K5MZA04	54-3	RSECAE	31-0
K5MZC04	54-3	RSECBA	31-0
K5MZE04	54-3	RSPCLE	31-0
LCTRKA	54-2	RTA190V	36-1
RAS330V	46-0	RTESTE	31-0
RCUETA	45-2	VKILM0	34-1
REPLA0V	42-0	VMILE0	34-1
RLADP0V	42-0	VRAZHE	34-1
RMRSTD4	53-0		
R0S030V	46-0		
R0S060V	46-0		
R0S070V	46-0		
ROUTS0V	45-2		
RWHIP0V	42-0		
R5MZBA	54-3		



FO-41. Front Panel Lamp Control Logic Diagram
(Sheet 1 of 4)

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
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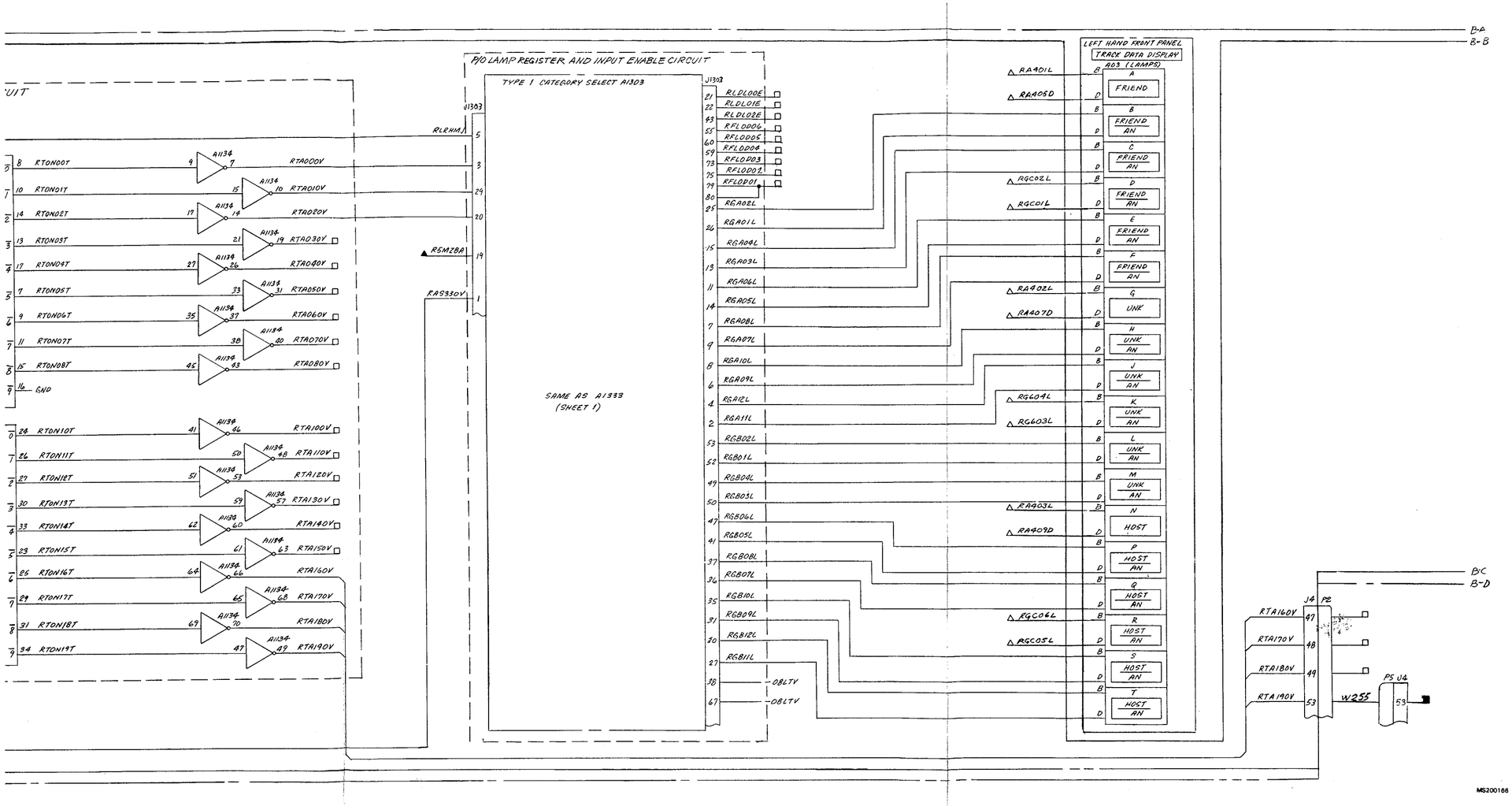
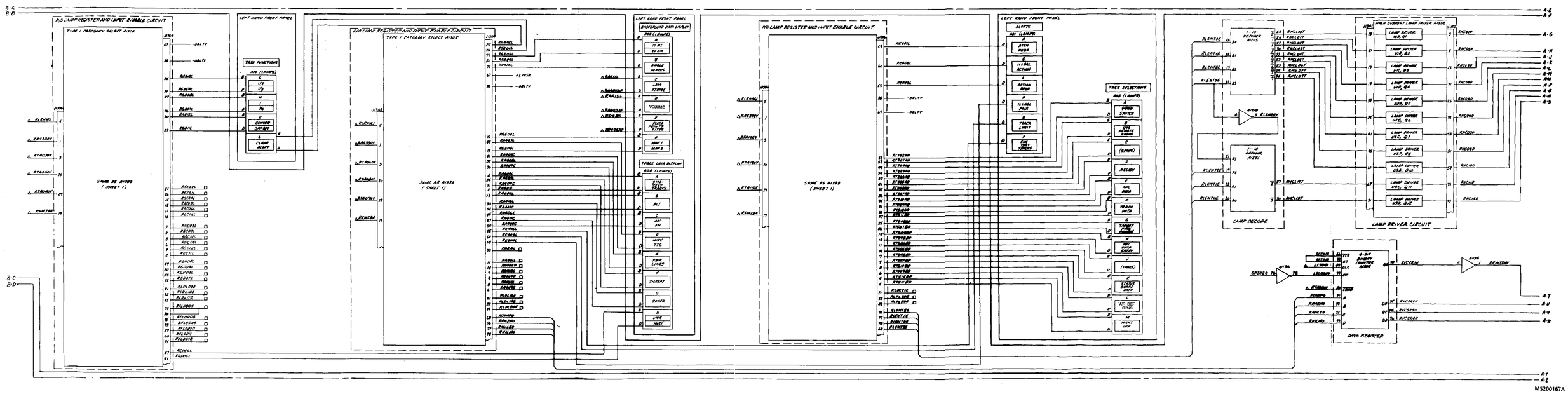
   □ OUTPUT TO SAME FIGURE

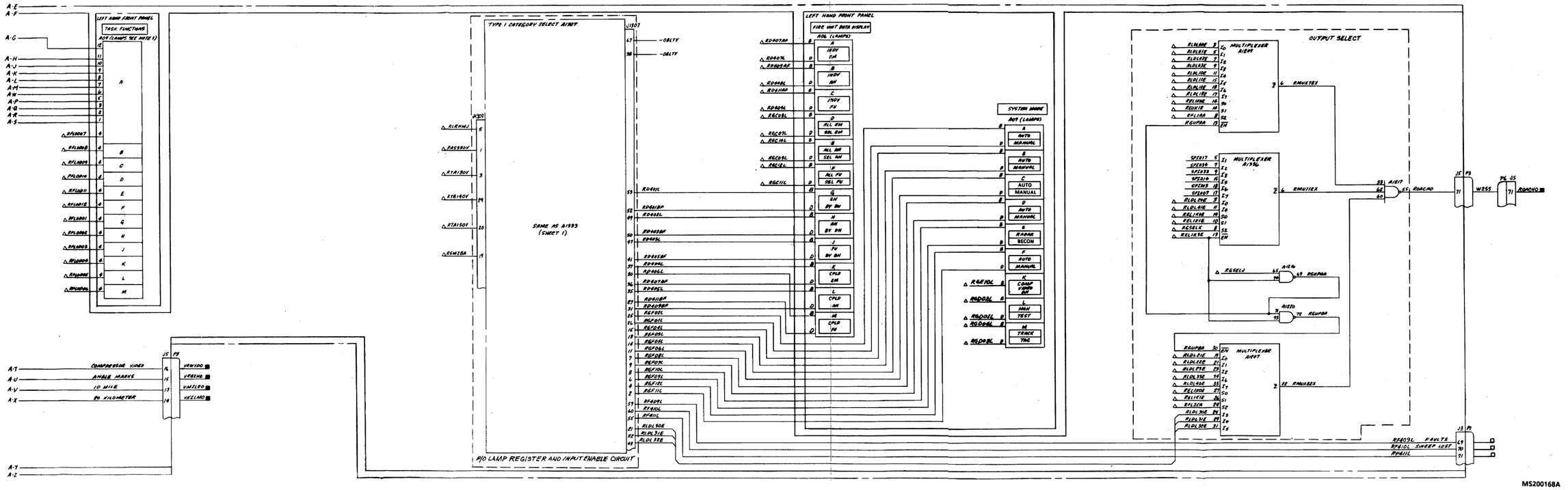
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.
9. [ ] INDICATES EQUIPMENT MARKINGS.
10. SWITCH A09 SEGMENTS A THRU M TERMINALS 1, 2, 3 AND 5 THRU 12 ARE CONNECTED TO RESPECTIVE TERMINALS OF SEGMENT A.



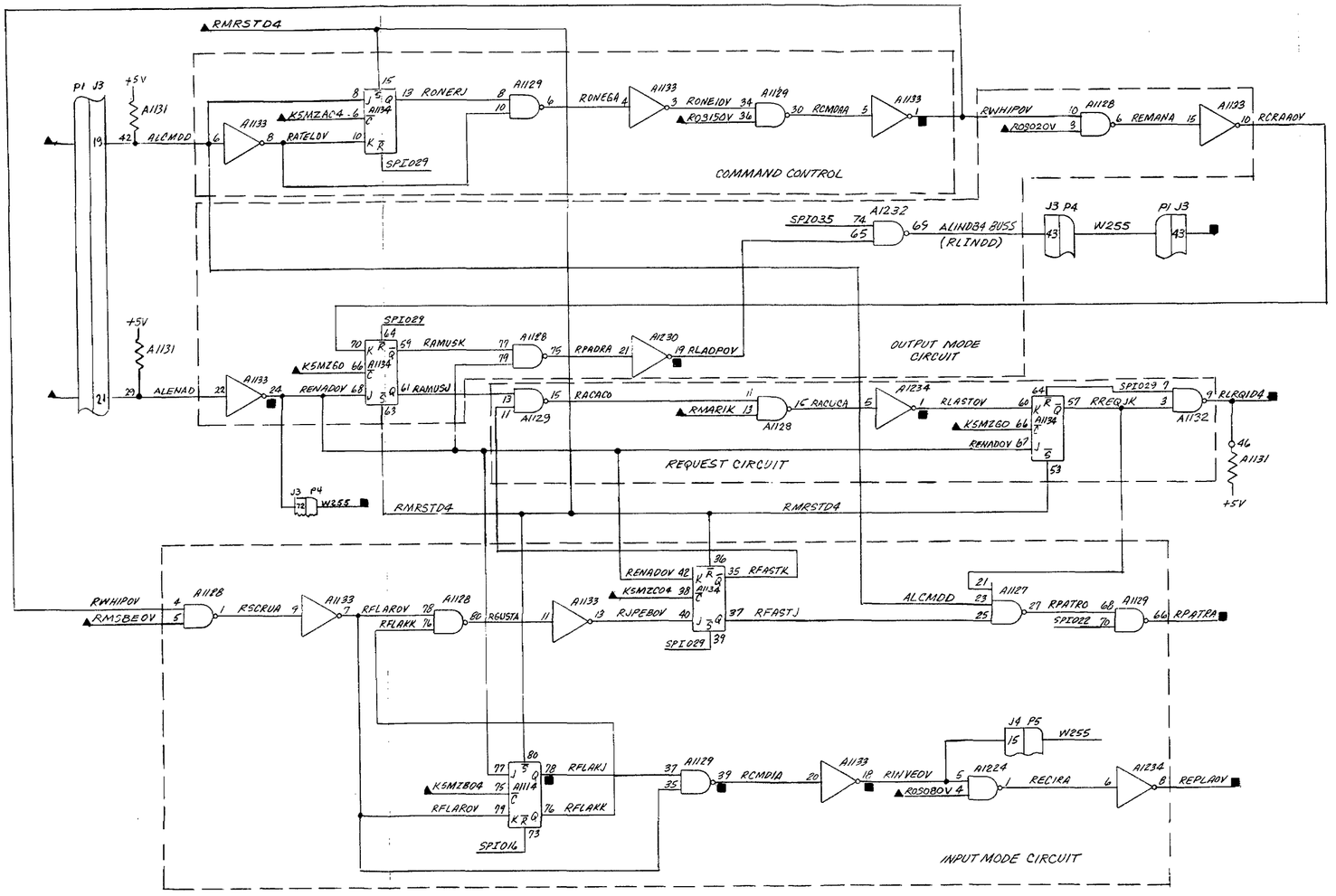
FO-41. Front Panel Lamp Control Logic Diagram (Sheet 2 of 4)



Change 1 FO-41. Front Panel Lamp Control Logic Diagram (Sheet 3 of 4)



Change 1 FO-41. Front Panel Lamp Control Logic Diagram (Sheet 4 of 4)



FO-42. Front Panel Input/ Output Control Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

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   △ INPUT FROM SAME FIGURE
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   □ OUTPUT TO SAME FIGURE

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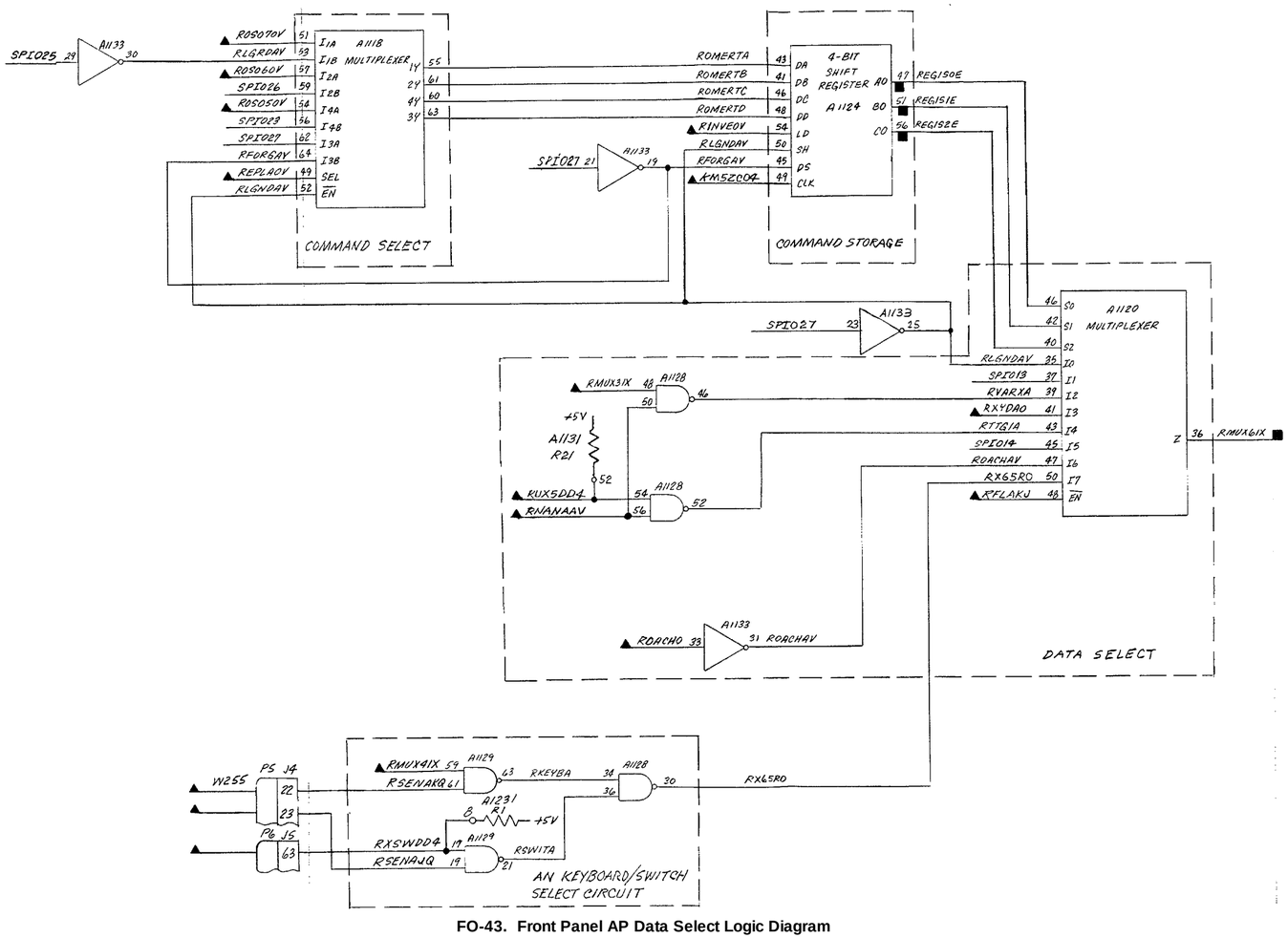
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.



NOTES: UNLESS OTHERWISE SPECIFIED

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2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

FO-43. Front Panel AP Data Select Logic Diagram

INPUTS	F/O – SH	OUTPUTS	F/O – SH
A3M2E04	54-2	RSENA3Q	43-0
KMS5TBA	53-0	RSENA3Q	43-0
R3M2BA	54-2		45-3
R3EGEK	45-3	RX3WDD4	43-0
R3G100E	43-0		
R3G101E	43-0		
R3G105E	43-0		
R3MAD0V	48-0		
R3MXL10V	48-2		
R3MXL00V	48-2		
R3MXE0V	48-2		
R3WBD0V	43-0		

CHART 1. SWITCH CODE TO SWITCH NOMENCLATURE CROSS REFERENCE

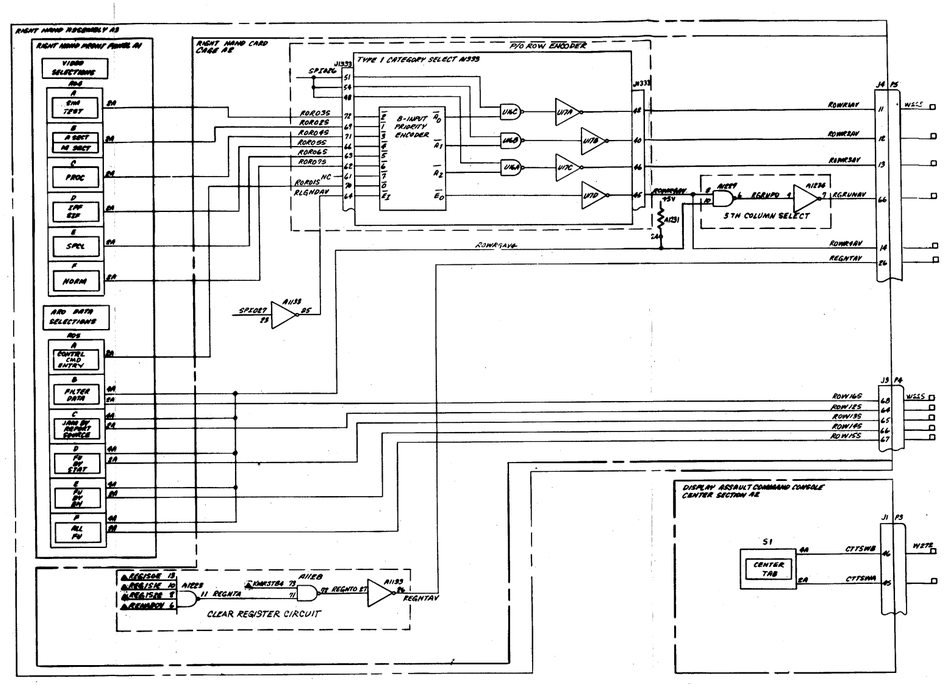
BINARY CODE COL	ROW	SWITCH CODE (DECIMAL)	SWITCH NOMENCLATURE
000	0001	1	FRIEND/AM (ATHR-TOR) A3B
000	0010	2	FRIEND/AM (OTHER REBY) A3C
000	0011	3	FRIEND/AM (LOCAL AUTO) A3E
000	0100	4	FRIEND/AM (LOCAL MANUAL) A3F
000	0101	5	UNK/AM (ATHR-TOR) A3H
000	0110	6	UNK/AM (OTHER REBY) A3J
000	0111	7	UNK/AM (LOCAL AUTO) A3L
000	1000	8	UNK/AM (LOCAL MANUAL) A3M
000	1001	9	HOST/AM (ATHR-TOR) A3P
000	1010	10	HOST/AM (OTHER REBY) A3Q
000	1011	11	HOST/AM (LOCAL AUTO) A3R
000	1100	12	HOST/AM (LOCAL MANUAL) A3T
000	1101	13	FRIEND/AM (Q73-RR) A3D
000	1110	14	UNK/AM (Q73-RR) A3K
000	1111	15	HOST/AM (Q73-RR) A3R
001	0000	16	ALL FRIEND, BN A4C
001	0001	17	ALL UNK, BN A4D
001	0010	18	ALL FRIEND, FU A4F
001	0011	19	MON/TEST (CONSOLE MODE) A7L
001	0100	20	TRACK/TAC (CONSOLE MODE) A7M
001	0101	21	UNK/HOST A4H
001	0110	22	1 / 1/4 A10H
001	0111	23	1/2 / 1/8 A10G
001	1000	24	CENTER/OFFSET A10K
001	1001	25	CLEAR ALERT A10L
001	1010	26	MAP 1/MAP 2 A2F
001	1011	27	FRIEND (VEL VECTOR) A3A
001	1100	28	UNK (VEL VECTOR) A3C
001	1101	29	HOST (VEL VECTOR) A3N
001	1110	30	BIB-TEST TRACKS A4A
001	1111	31	ALT A4C
010	0000	32	AIR SPEED A4E
010	0001	33	ADR, DATA A4G
010	0010	34	PAIR LINES A4E
010	0011	35	THREAT A4F
010	0100	36	SPEED A4G
010	0101	37	JAM STROBE A3C
010	0110	38	VOLUME A2D
010	0111	39	FIXED POINTS SITES A2E
010	1000	40	TARGET PROC PARAM A8G
010	1001	41	PPI DATA ENTRY A8H
010	1010	42	(SPARE)
010	1011	43	STATUS BOARD DATA A8K
010	1100	44	AIR DEF OPNS A8L
010	1101	45	IDENT IFF A8M
010	1110	46	VIDEO SWITCH A8A
010	1111	47	Q73-REMOTE RADAR A8B
011	0000	48	(SPARE)
011	0001	49	ADR, BN A8E
011	0010	50	ADR, DATA A8E
011	0011	51	TRACK DATA A8F
011	0100	52	(SEE CHART 2)
011	0101	53	(SEE CHART 2)
011	0110	54	(SEE CHART 2)
011	0111	55	(SEE CHART 2)
011	1000	56	(SEE CHART 2)
011	1001	57	(SEE CHART 2)
011	1010	58	(SEE CHART 2)
011	1011	59	(SEE CHART 2)
011	1100	60	(SEE CHART 2)
011	1101	61	(SEE CHART 2)
011	1110	62	(SEE CHART 2)
011	1111	63	(SEE CHART 3)
100	0000	64	(SPARE)
100	0001	65	A SECTR SECT A4B
100	0010	66	BIB/TEST A4A
100	0011	67	PROC A4C
100	0100	68	IFF-SIF A4D
100	0101	69	SPCL A4E
100	0110	70	NORM A4F
100	0111	71	(SPARE)
100	1000	72	(SPARE)
100	1001	73	(SPARE)
100	1010	74	(SPARE)
100	1011	75	JAM BY REPORT SOURCE A5C
100	1100	76	FU BY STAT A5D
100	1101	77	FU BY BN A5E
100	1110	78	ALL FU A5F
100	1111	79	ALT BY DATA A5B
101	0000	80	10 MI/20 KM A2A
101	0001	81	ANGLE MARKS A2B
101	0010	82	COMP VIDEO ON (CONSOLE MODE) A7K
101	0011	83	AUTO/MANUAL (HOLDFIRE) A7A
101	0100	84	AUTO/MANUAL (ASSIGN) A7B
101	0101	85	AUTO/MANUAL (CLASSIFIED) A7C
101	0110	86	AUTO/MANUAL (INITIATE) A7D
101	0111	87	RADAR/BEACON (TRACE) A7E
101	1000	88	AUTO/MANUAL (INTRG) A7F
101	1001	89	EM BY BN A4G
101	1010	90	AN BY BN A6H

CHART 1. SWITCH CODE TO SWITCH NOMENCLATURE CROSS REFERENCE

BINARY CODE COL	ROW	SWITCH CODE (DECIMAL)	SWITCH NOMENCLATURE
101	1011	91	FU BY BN A5J
101	1100	92	(SPARE)
101	1101	93	(SPARE)
101	1110	94	(SPARE)
101	1111	95	INDV EM A6A
110	0000	96	INDV AN A6B
110	0001	97	INDV FU A6C
110	0010	98	CEASE FIRE (TERMN COMMANDS) A7G
110	0011	99	HOLD FIRE (TERMN COMMANDS) A7H
110	0100	100	CEASE ENGAGE (TERMN COMMANDS) A7J
110	0101	101	DESIG OFFSET A10J
110	0110	102	DROP A10M
110	0111	103	DESIG MODE A10A
110	1000	104	DEHOOK A10B
110	1001	105	NUMBER HOOK A10C
110	1010	106	SEQ HOOK A10D
110	1011	107	UPDATE A10E
110	1100	108	INITIATE A10F
110	1101	109	CENTER TAB S1
110	1110	110	(SPARE)
110	1111	111	ATTN REQD A1A
111	0000	112	ILLEGL ACTION A1B
111	0001	113	ACTION REQD A1C
111	0010	114	ILLEGL PAIR A1D
111	0011	115	TRACK LIMIT A1E
111	0100	116	SIM TEST TRACKS A1F
111	0101	117	(SPARE)
111	0110	118	(SPARE)
111	0111	119	(SPARE)
111	1000	120	(SPARE)
111	1001	121	(SPARE)
111	1010	122	(SPARE)
111	1011	123	(SPARE)
111	1100	124	(SPARE)
111	1101	125	(SPARE)
111	1110	126	(SPARE)
111	1111	127	(SPARE)

CHART 2. TABS FUNCTION DIAGRAM

BIN CODE	TRACK TABS	DATA TABS	ASSIGN	SPARE	SECTR SECT TABS	VIDEO SWITCH	IFF SIF	AIR DEF OPNS	SPARE	SPARE	PPI DATA ENTRY	TARGET PROC PARAM
	TABS SELECTIONS											
	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11	S12
63	•	WEAPON TYPE	ACCEPT RECVD ASSIGN		LINK 9	DEMO MAP 1	FRIEND	MODE CHAL	ASSIGN NOW NUMBER		ENTER ALT LIMITS	START RANGE
62	TRACK HEIGHT	ADL ADDR	•		LINK 8	DEMO SPCL VIDEO	UNK	CMD CODE	•		ENTER THREAT LIMIT	STOP AT RANGE
61	TRACK VEL HDG	•	SIN ASSIGN		LINK 7	DEMO VPU-A INPUT	UNK AMD/MD ENEMY	COMPU CODE	FU FLIGHT STATUS		DJSG ENTER FU	GATE COM-PLETE
60	POINT ENTRY	SAMD PTR	ENGAGE		LINK 6	DEMO VPU-B INPUT	HOST	ACTION CLEARG CODE	FU STATUS		DESIG DEV AN	•
59	SITE INIT-IDENT	•	L/GAGE RD/YLE		LINK 5	ECCM 2	IDENT/ AMPLI-CT-PLT	SEND PTR	SEL COUNT HOT		DESIG DEV UNK	•
58	SITE ADDR-RABLE	•	CLEAR EFFECT		JAMMD PUS	ECCM 1	IDENT/ TEST IDENT	DROP PTR	SEL COUNT COLD		DESIG DROP VECTOR	G SIMU-TNEITY
57	RAID SIZE WHOLE	COMPLE CODE	CLEAR STATUS		LINK 10	DEMO MAP 2	IFF MODE DEMO	INTER-ROGATE	•		ENTER SPEED LIMITS	PROC NORMAL
56	RAID SIZE FEW	ACTION MAMAGE CODE	CANCEL REC ASSIGN		LINK 11	NORM-AL VIDEO	INTER-ROGATE	FRIEND	•		DESIG ENEMY	PROC INT 1
55	RAID SIZE MANY	CMD CODE	•		LINK 12	MTI VIDEO	MODE CHAL	UNK	•		DESIG FU BY BN	CEMSCR
54	AUTO-RAMTP	DROP PTR	•		•	GATED MTI VIDEO	ENTER IFF MODE CODE	HOST	•		DESIG AN BY BN	RETURN TO AUTO
53	ENTER JAM STROBE	•	•		LINK 13	ECCM 3	•	ENGAGE	MSLS DE-FENDED		DESIG FU BY BN	•
52	CHASE JAM STROBE	•	CLEAR HOLD FIRE		•	ECCM 4	TIM	ACCEPT RECVD ASSIGN	•		CLEAR DESIG VECTOR	INTER-ROGATE MODE



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AN ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE A FOLLOWS:
   - ▲ INPUT FROM ANOTHER FIGI
   - △ INPUT FROM SAME FIGURE
   - ■ OUTPUT TO ANOTHER FIGU
   - ◪ OUTPUT TO BOTH SAME AN
   - ◪ OUTPUT TO SAME FIGURE
   - □
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTA AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER A GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIOI AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.
9. INDICATES EQUIPMENT MARKING

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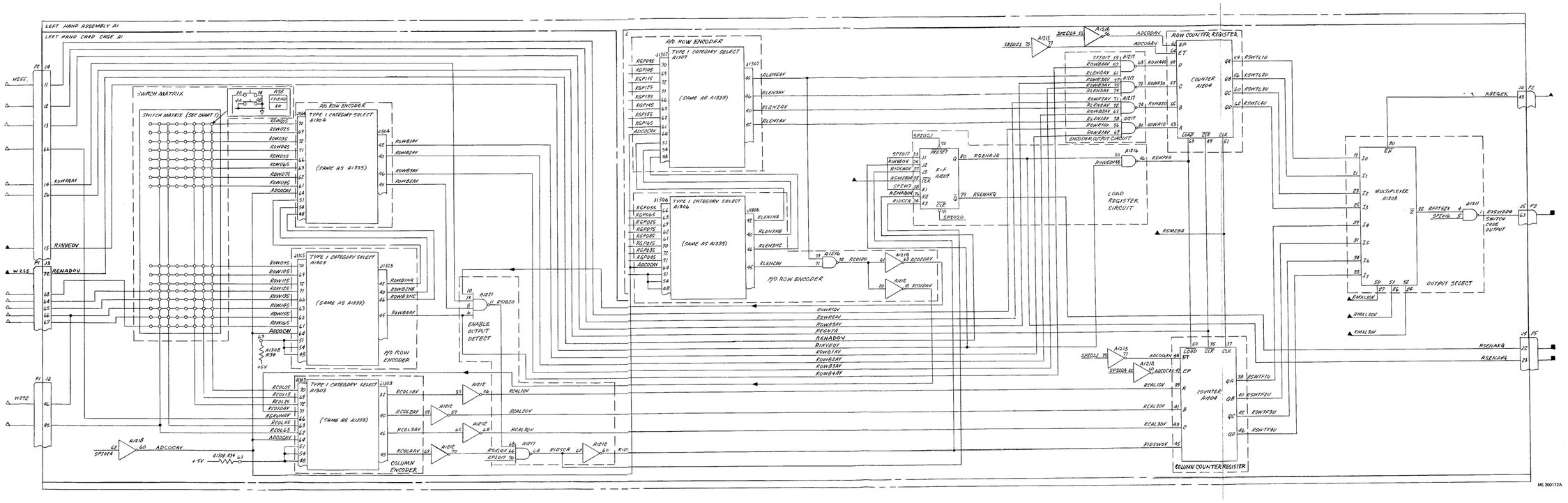
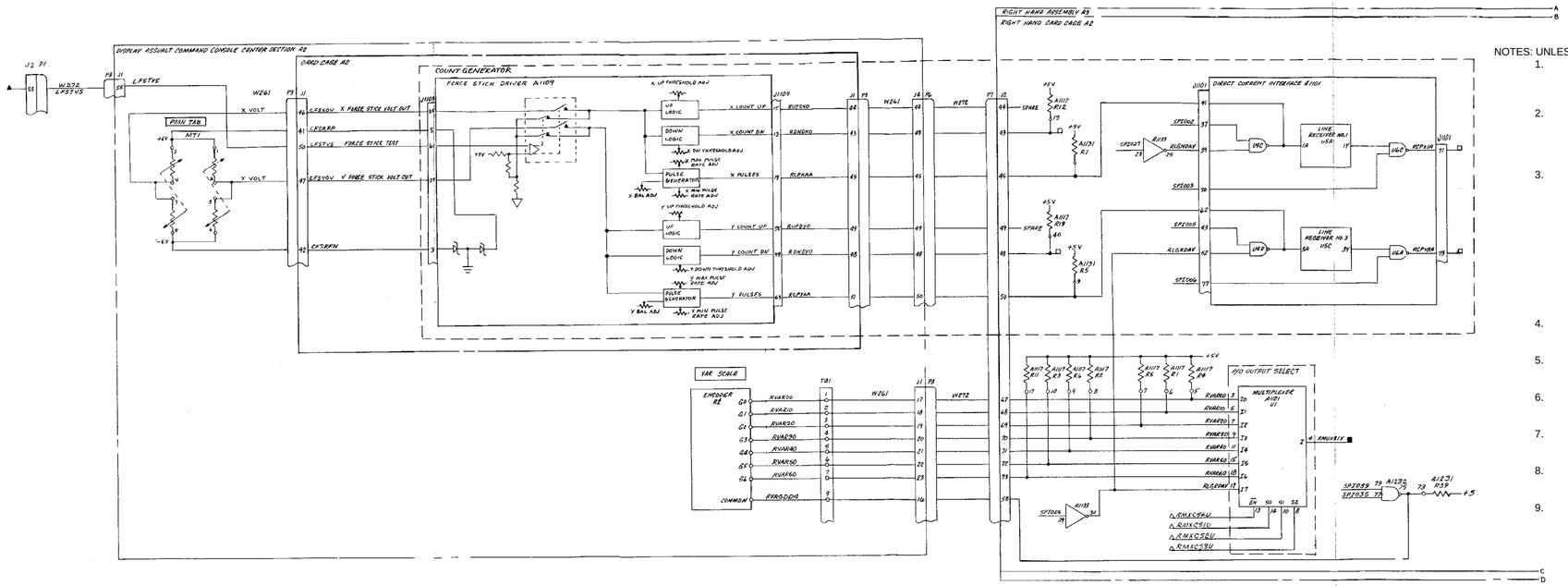
CHANGE 1 FO-44. Front Panel Switch Coding Logic Diagram (Sheet 1 of 2)



FO-44. Front Panel Switch Coding Logic Diagram
(sheet 2 of 2)

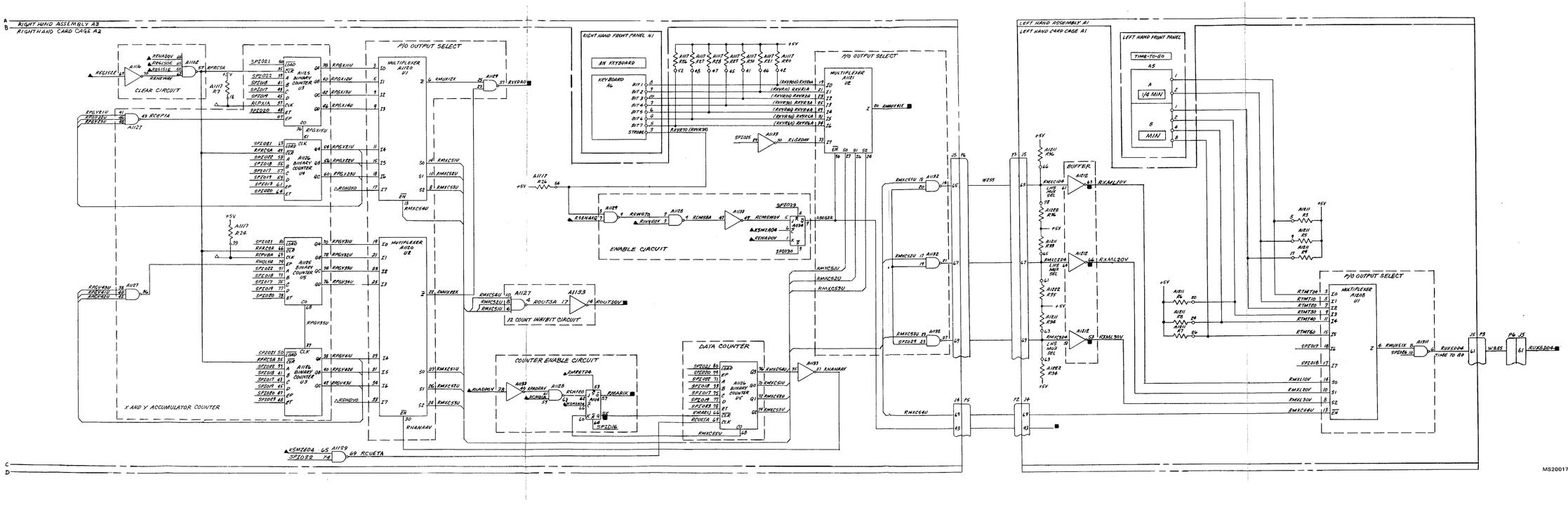


INPUTS	F/O - SH	OUTPUTS	F/O - SH
KSMZA04	54-3	RBRGEK	44-2
KSMZE04	54-2	RCUETA	41-1
LFSTVS	49-3	RMAR1U	48-0
NCMDIA	42-0	RMAR1K	42-0
REG150E	43-0	RMUX31X	43-0
REG151E	43-0	RMUX41X	43-0
REG152E	43-0	RSUTS0V	41-2
RENAD0V	42-0	RUXSDD4	43-0
RLAD0VV	42-0	RXM110V	44-2
RMRSTD4	53-0	RXM120V	44-5
RSENAKQ	44-2	RXM130V	44-2
RLNVE0V	42-0	RXYDA0	43-0

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:
   - ▲ INPUT FROM ANOTHER FIGURE
   - △ INPUT FROM SAME FIGURE
   - ■ OUTPUT TO ANOTHER FIGURE
   - ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   - □ OUTPUT TO SAME FIGURE
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.
9. ▭ INDICATES EQUIPMENT MARKING

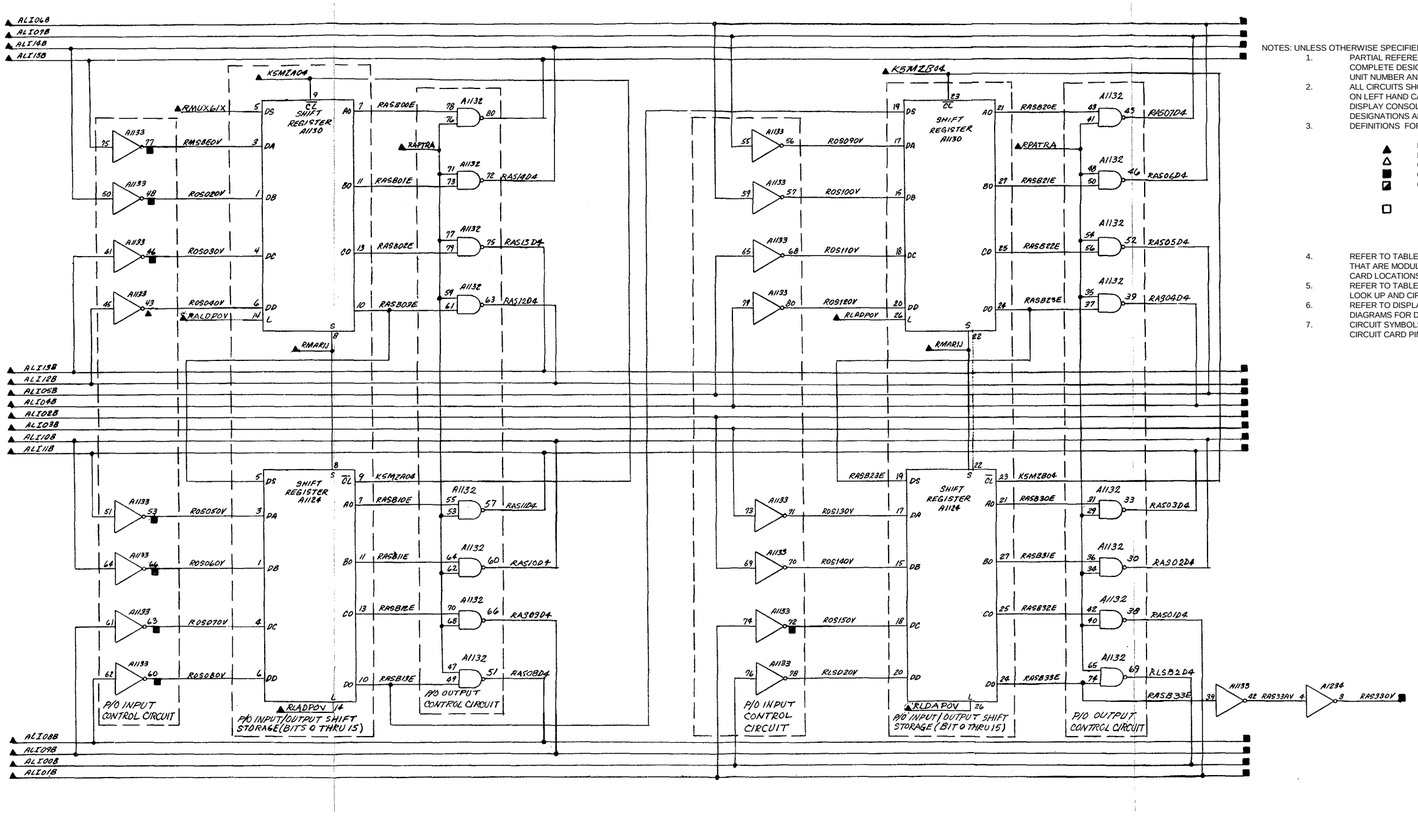
FO-45. Front Panel Data Multiplexing Logic Diagram (sheet 1 of 2)



FO-45. Front Panel Data Multiplexing Logic Diagram
(Sheet 2 of 2)

INPUTS	F/O - SH
AL000B	5-0
AL001B	5-0
AL002B	5-0
AL003B	5-0
AL004B	5-0
AL005B	5-0
AL006B	5-0
AL007B	5-0
AL008B	5-0
AL009B	5-0
AL010B	5-0
AL011B	5-0
AL012B	5-0
AL013B	5-0
AL014B	5-0
AL015B	5-0
KSMZA04	54-3
KSMZB04	54-3
RLADP0V	42-0
RMAR1J	45-2
RMUX61X	43-0
RPATRA	42-0

OUTPUTS	F/O - SH
AL000B	5-0
AL001B	5-0
AL002B	5-0
AL003B	5-0
AL004B	5-0
AL005B	5-0
AL006B	5-0
AL007B	5-0
AL008B	5-0
AL009B	5-0
AL010B	5-0
AL011B	5-0
(RAS11D4)	
AL012B	5-0
(RAS12D4)	
AL013B	5-0
(RAS13D4)	
AL014B	5-0
AL015B	5-0
RAS330V	41-1
RAS833E	36-1
RMSBE0V	42-0
R06020V	42-0
R06030V	41-2
R06050V	43-0
R06060V	41-2
	43-0
R06070V	41-2
	43-0
R06080V	42-0
R06150V	42-0



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIG
   ◪ OUTPUT TO SAME FIGURE
   □

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.

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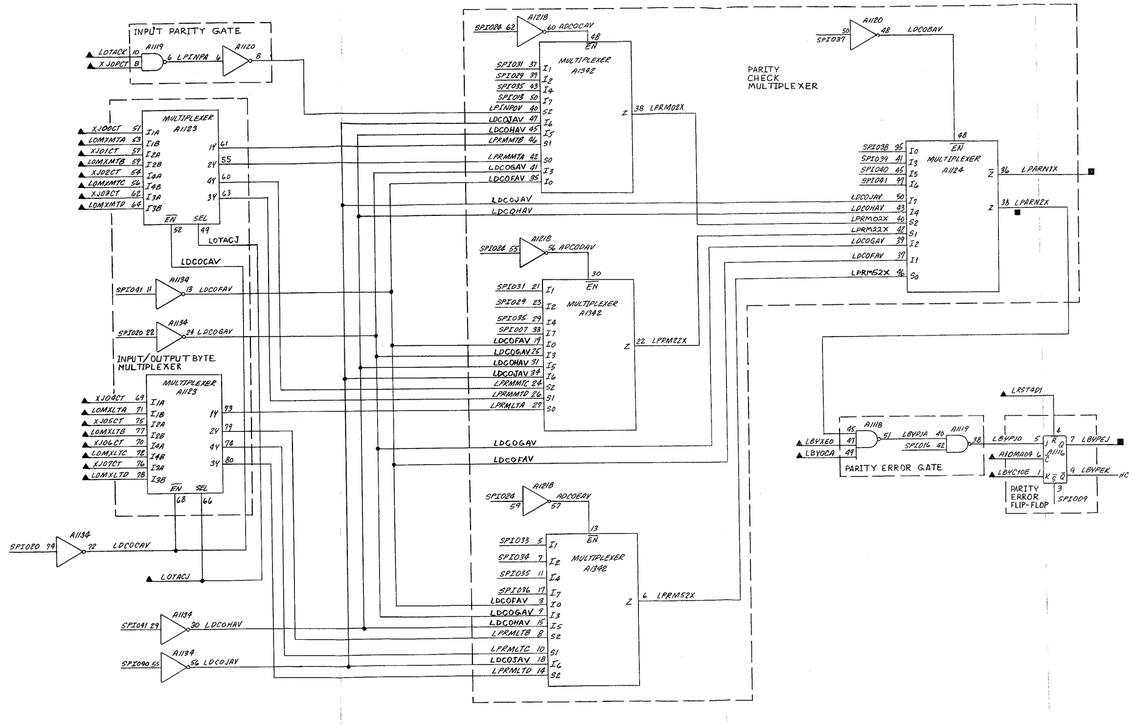
FO-46. Front Panel Input/Output Data Buffer Register Logic Diagram

INPUTS	F/O - SH	INPUTS	F/O - SH
A16MA04	54-2	L0TACJ	51-0
LBYC10E	51-0	L0TACK	51-0
LBY0CA	51-0	LBST4D1	53-0
LBYXE0	51-0	XJ0PCT	48-1
L0MXLTA	48-1	XJ00CT	48-1
L0MXLTB	48-1	XJ01CT	48-1
L0MXLTC	48-1	XJ02CT	48-1
L0MXLTD	48-1	XJ03CT	48-1
L0MXMTA	48-1	XJ04CT	48-1
L0MXMTB	48-1	XJ05CT	48-1
L0MXMTC	48-1	XJ06CT	48-1
L0MXMTD	48-1	XJ07CT	48-1

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
LBYPEJ	51-0	LPARN1X	48-1
LPARN1X	51-0		



FO 47. Computer Buffer/C-BIT Parity Generation Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

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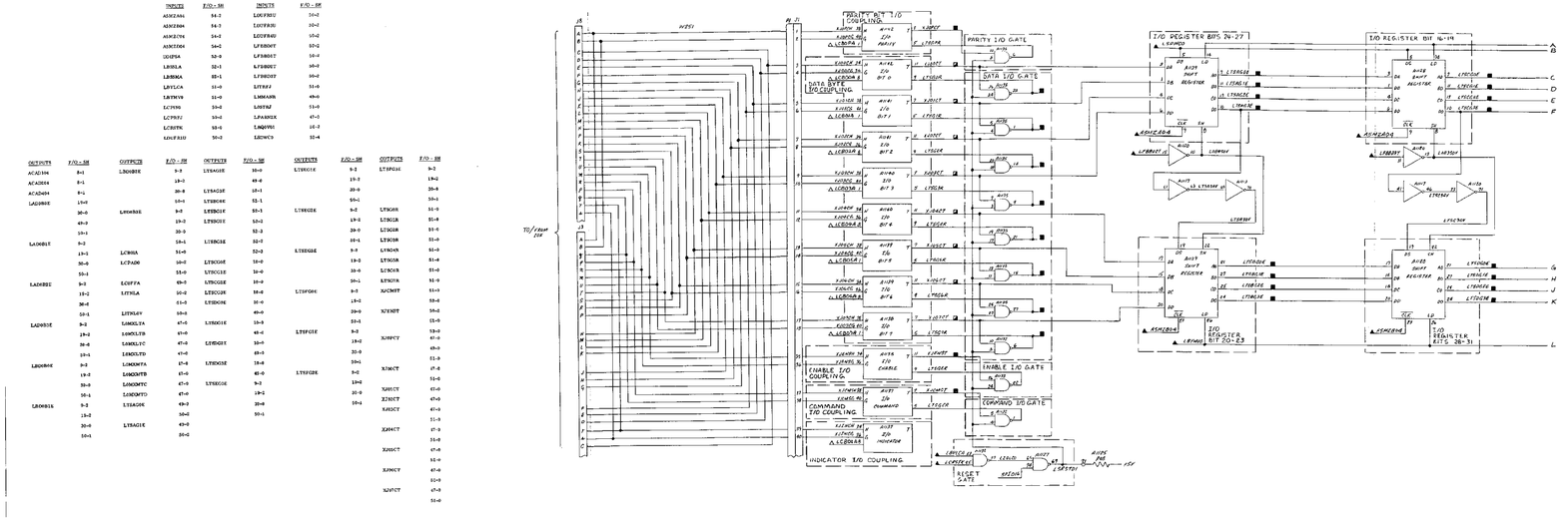

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN , FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
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5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.
9. ▭ INDICATES FRONT PANE; MARKING

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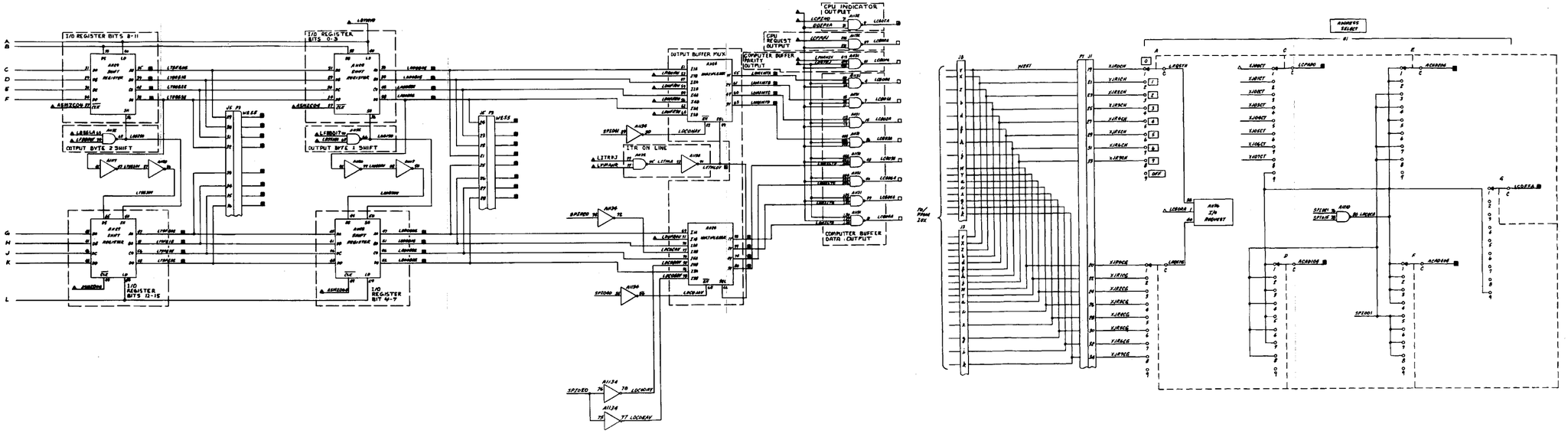
FO-48. Computer Buffer/C-BIT Input/Output Register Logic Diagram (Sheet 1 of 2)



Change 1 FO-48. Computer Buffer/C-BIT Input/Output Register Logic Diagram (Sheet 2 of 2)

INPUTS	I/O - SH	INPUTS	I/O - SH
A1EMA04	54-2	LCBITX	53-3
A6EEC04	54-2	LCTEKA	54-2
A6NEI04	54-2	L0VDMV	16-1
A6NEI04	54-2	L0VRGO	51-4
EDCTBA	16-2	L3BTI01	53-3
L4D0002	48-1	L3BTI01	53-3
L4D002L	53-3	L3BT401	53-3
LAPTBA	8-2	LTEAGIE	48-1
LBITOOV	48-2	LTEAGIE	48-1
LBR00L	50-1	LTEAGIE	48-1
LBTEEQ	48-5	LTEOOIE	48-1
LBTC11E	51-6	LTEOOIE	48-1
LBTEIB	51-6	LTEOOIE	48-1
LBTEOV	51-6	LTEOOIE	48-1
LBTCOV	51-6	XMPCT	48-1
LCST7A	48-2		

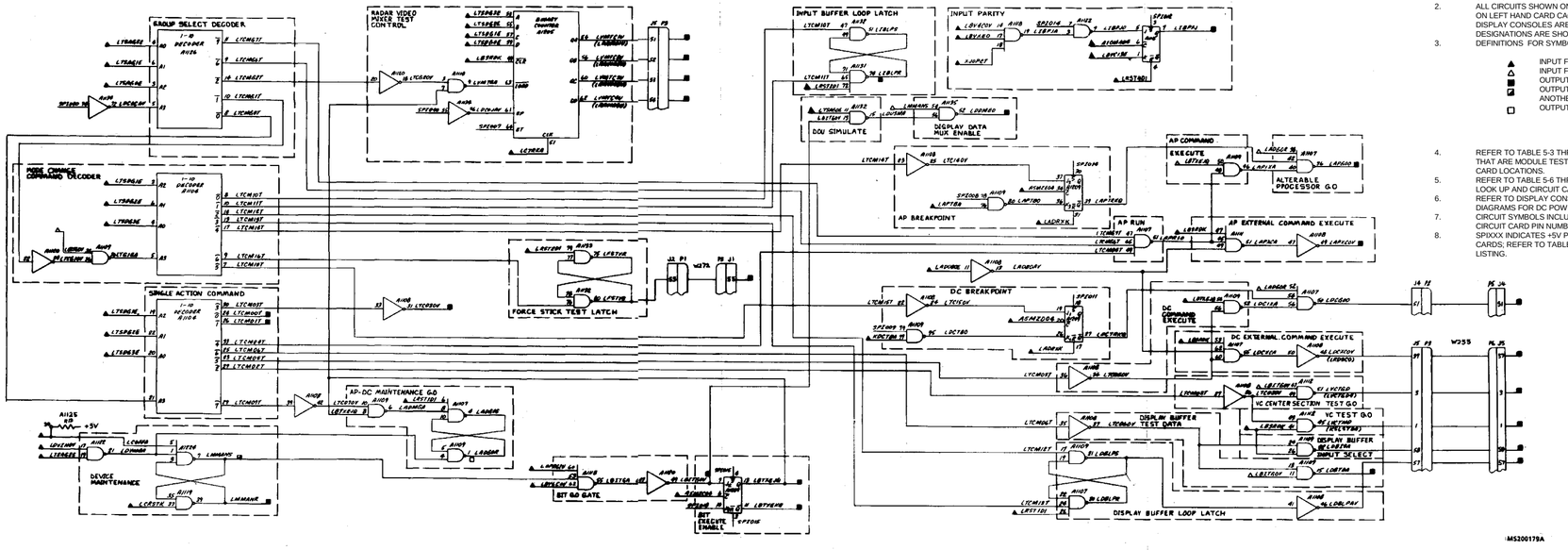
OUTPUTS	I/O - SH	OUTPUTS	I/O - SH
LBITOO (ISOLATED)	35-2	LBRPJ	1-2
	35-2	LBRAMR	48-1
	35-1		36-2
LAPO08	36-2	LBRAMR	1-2
	16-1		36-2
LAPEOV (LOOC)	8-2		51-2
LBITOOV	48-1	LBRCO	13-2
	48-2	LTCIBBT	35-1
	35-2	LTCIBBT	35-1
LBTEEQ	35-1	LTCIBBV	36-2
LBTEEBQ	35-1	LTCTBB (LTCTEBQ)	34-2
LBRBA	35-2	LTCTBB (LTCTEBQ)	35-2
LBRLPAY	35-2		35-2
LBCO08	35-2	LBITCIC (LBATEBB)	35-2
	35-2	LBITCIC (LBATEBB)	35-2
LBRR08	51-2	LBITCIC (LBATEBB)	35-2
LPBTYE	48-1	LBITCIC (LBATEBB)	35-2
LBRLPB	6-2	LBITCIC (LBATEBB)	35-2

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

▲ INPUT FROM ANOTHER FIGURE
△ INPUT FROM SAME FIGURE
■ OUTPUT TO ANOTHER FIGURE
◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
□ OUTPUT TO SAME FIGURE

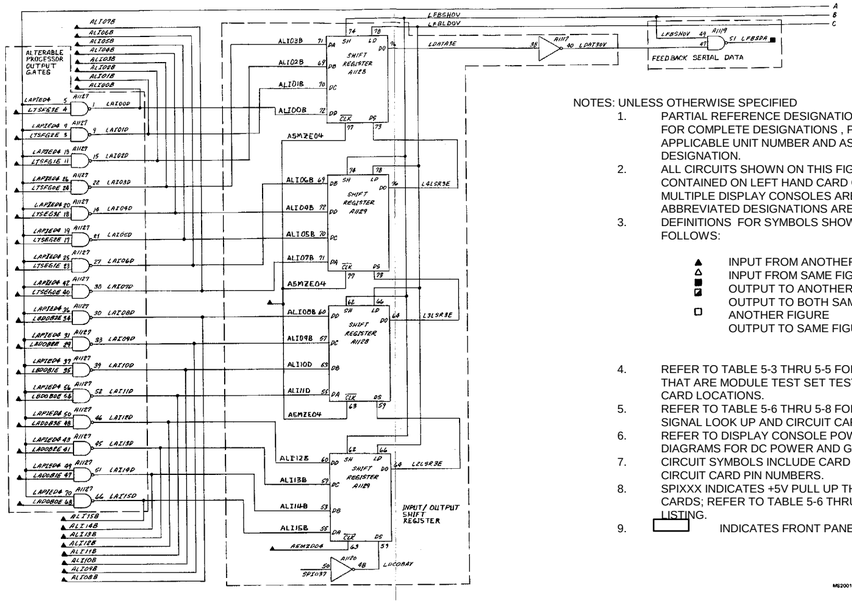
4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.



Change 1 FO-49. Computer Buffer/C-BIT Test Decoding Logic Diagram

INPUTS	F/O – HH	INPUTS	F/O – II	INPUTS	F/O – JJ
AIBCAK	4-1	LADSBI1E	46-1	LSPBGH3U	51-0
ALCMIG	5-0	LADSBI2E	46-1	LSRT8J	51-0
ALENFJ	5-0	LADSBI3E	46-1	LSSDEK	53-0
ALI0CB	5-0	LASPAC6V	5-0	LSSTSD1	53-0
ALI01B	5-0	LASPJA	5-0	LSSTSD1	53-0
ALI07B	5-0	LBOSBK6E	45-1	LSSTSD1	53-0
ALI03B	5-0	LDD4B21E	45-1	LTEAG5E	48-1
ALI04B	5-0	LDD4B22E	45-1	LTEAG1E	48-1
ALI05B	5-0	LBO4B3E	45-1	LTEEG5E	48-1
ALI0ND	5-0	LB0E2U	52-1	LTEEG1E	48-1
ALI07B	5-0	LBYC18E	51-0	LTEEG2E	48-1
ALI06D	5-0	LBYC31E	51-0	LTEEG3E	48-1
ALI09B	5-0	LBYT1JQ	51-0	LTEFG5E	48-1
ALI02B	5-0	LBYWC6V	51-0	LTEFG1E	48-1
ALI11B	5-0	LCPAD6	48-2	LTEFG2E	48-1
ALI12B	5-0	LCRWTK	52-0	LTEFG3E	48-1
ALI13B	5-0	LCTBEA	54-2	XJENBT	46-1
ALI14B	5-0	LFBLBA	51-0		
ALI15B	5-0	LIFBLA	48-1		
A8W6U	13-0	LITHGAV	46-1		
A8W98K	13-0	LITRPJ	51-0		
ASMZA04	54-2	LMMANH	49-0		
ASMZC04	54-2	LMMANS	49-0		
ASMZD04	54-2	LMSBTK	53-0		
ASMZE04	54-2	LSPEBAY	51-0		
LADOBOE	46-1	LSPBGH3U	51-0		

OUTPUTS	F/O – KK	OUTPUTS	F/O – RR
ALIN0N4	5-0	LFNADNV	51-0
LCFIBK	46-1	LFSBD0T	46-1
LCPBFJ	48-2	LFSBD1T	46-1
LDC0BA	53-0	LFSBD2T	46-1
LDG0N0V	8-2	LFSBD3T	46-1
LDNQAAV	8-1	LFSBDJ	51-0
LDCFB2U	48-1	LFSBDA	52-4
LDCF32U	48-1	LMFEC6V	8-2
LDCF52U	48-1	LMFED6V	8-2
LDCF54U	48-1	LMT0A6V	8-2
LGVIN0V	48-0	LNQ6VG1	8-1
LGVSPA	53-0		48-1
LGVSP0V	53-0		


ALTERABLE PROCESSOR OUTPUT GATES
ALI07B
ALI06B
ALI05B
ALI04B
ALI03B
ALI02B
ALI01B
ALI00B
LADSBI0E
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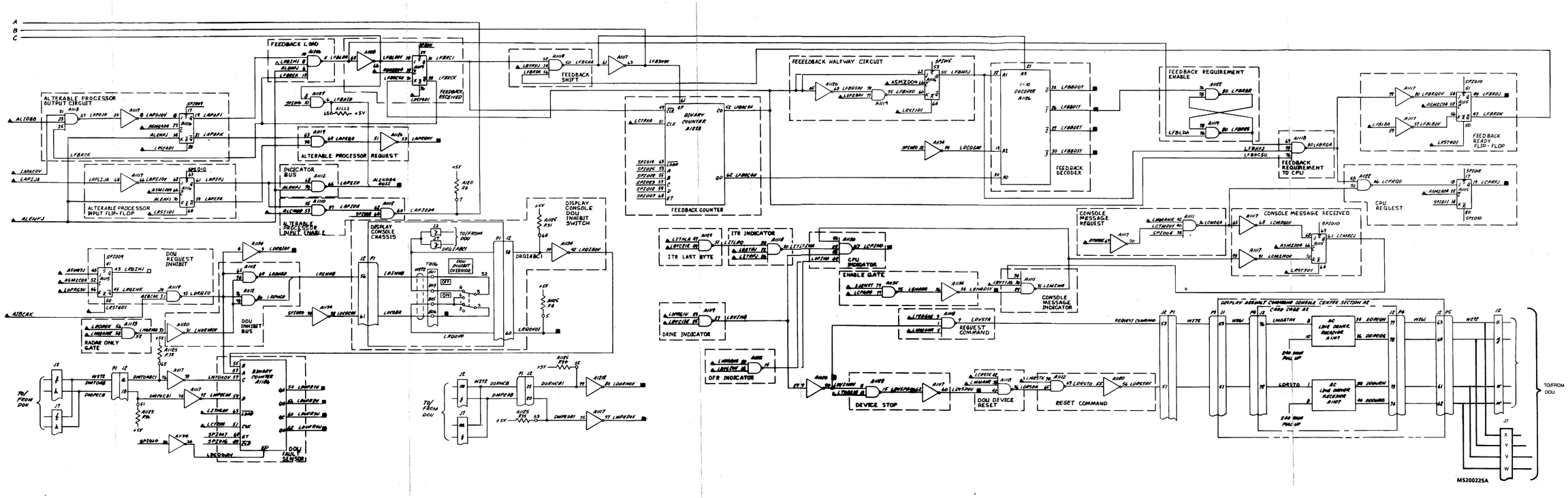
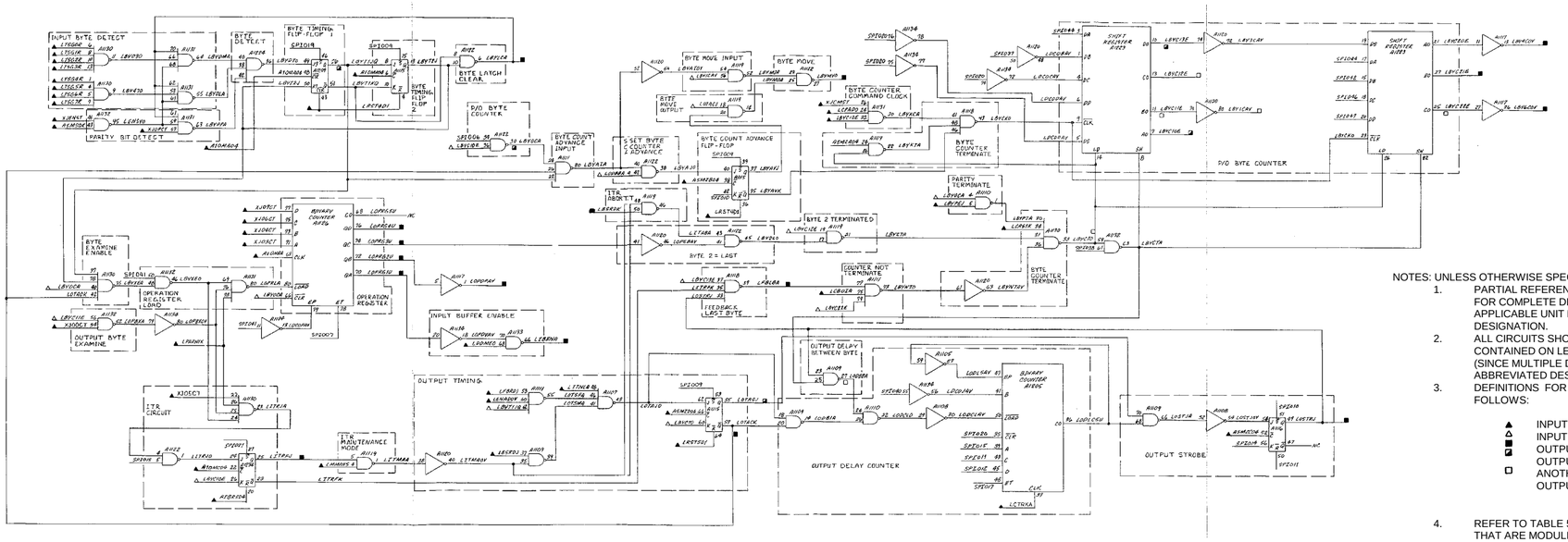


FO-50. Computer Buffer/C-BIT Alterable Processor and Display Output Unit Interface Logic Diagram (Sheet 2 of 2) Logic Diagram

INPUTS	F/O - SH	INPUTS	F/O - SH
A1BRDH	53-0	LMMANS	49-0
A1MAA4	54-2	LPARNUK	47-0
A1MC04	54-2	LBSTG1	53-0
A1NBA	54-2	LBSTG1	53-0
A1MSQK	54-2	LTSG2R	48-1
A1MZA4	54-2	LTSG1R	48-1
A1MZB4	54-2	LTSG2R	48-1
A1MZC4	54-2	LTSG3R	48-1
A1MZD4	54-2	LTSG4R	48-1
LBSRDJ	52-1	LTSG5R	48-1
LBSRDK	52-1	LTSG6R	48-1
LBYPAJ	47-0	LTSG7R	48-1
LCBRIA	48-1	XJCNDT	48-1
LCPAD0	48-2	XJENST	48-1
LCRSTK	53-0	XJ00CT	48-1
LDDMZ2	48-0	XJ00CT	48-1
LKNAGOV	50-2	XJ00CT	48-1
LPBRDJ	50-2	XJ00CT	48-1
LTTKLA	48-1	XJ00CT	48-1

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
LBYC1DE	47-0	LPRLBA	50-2
LBYC1SE	49-0	LIBENA	50-0
	50-2	LITRPJ	48-1
LBYC1SE	50-2		50-2
LBYLCA	48-1	LSPERAV	50-2
LBYMVD	48-1	LSPOFAV	52-1
LBYMCA	47-0	LSPRCSU	50-2
LBYTLJQ	50-2	LSPRCSU	49-0
LBYXE0	47-0	LSPRCSU	50-2
	48-0	LSPRCSU	53-0
LBYSCSV	49-0	LSSTRJ	48-1
LBYSCSV	49-0		50-2
	50-2	LOTACJ	47-0
		LOTACK	47-0



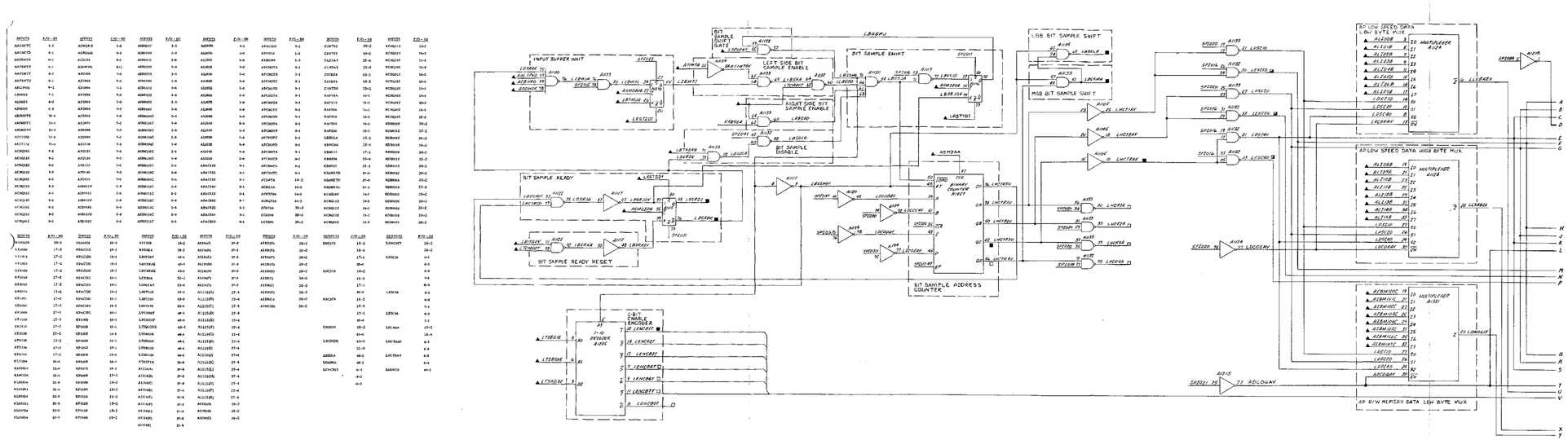
FO-51. Computer Buffer/CBIT Input/Output Control Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

4. REFER TO TABLE 5-3 THRU 5-5 FOR CIRCUIT CARDS THAT ARE MODULE TEST SET TESTABLE AND CIRCUIT CARD LOCATIONS.
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.



NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
   ■ OUTPUT TO ANOTHER FIGURE
   ◪ OUTPUT TO BOTH SAME AND ANOTHER FIGURE
   □ OUTPUT TO SAME FIGURE

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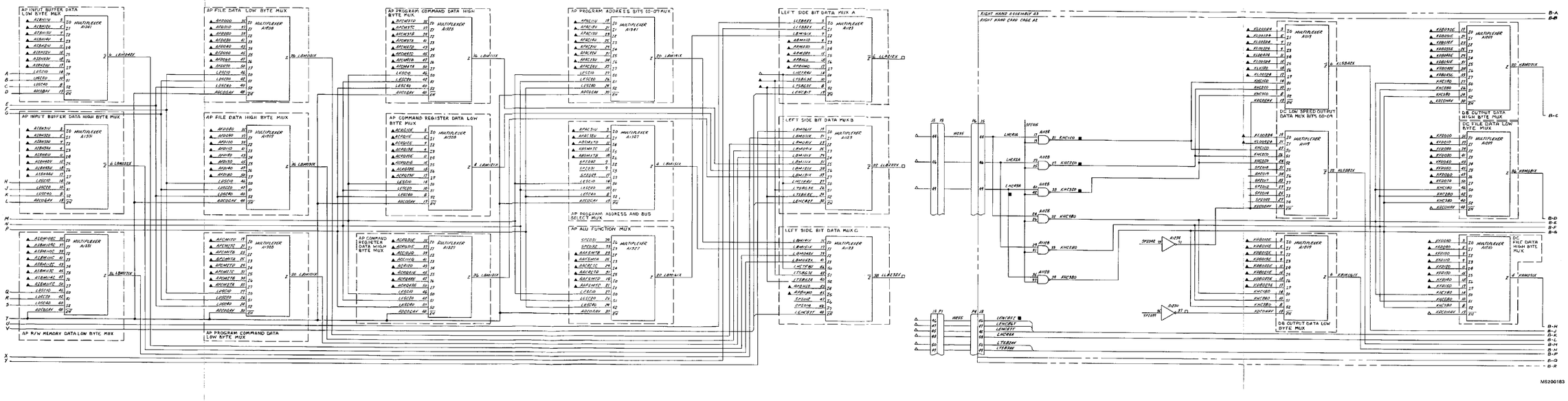
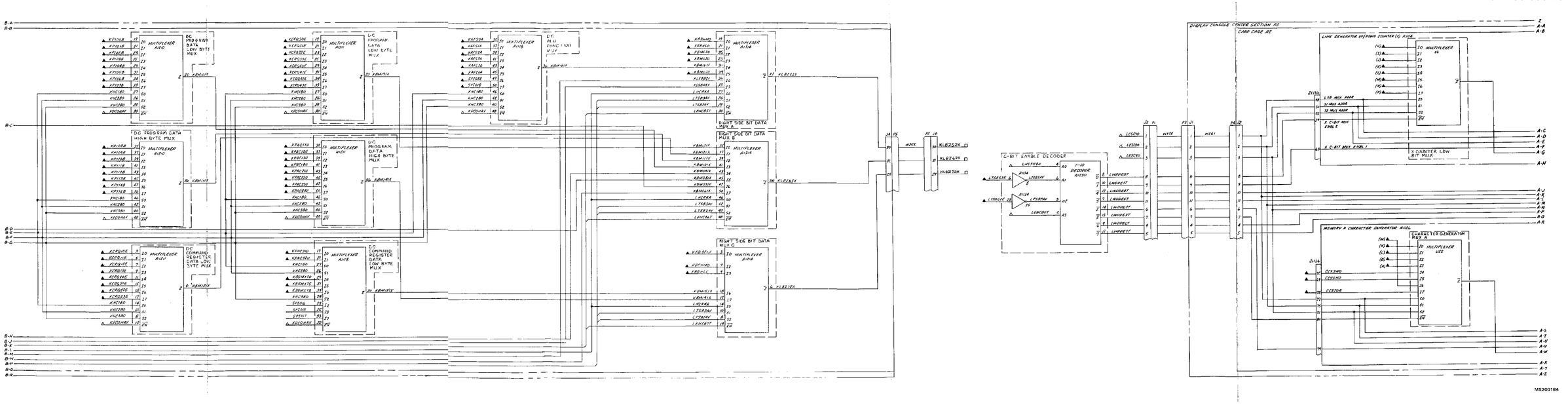
5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.

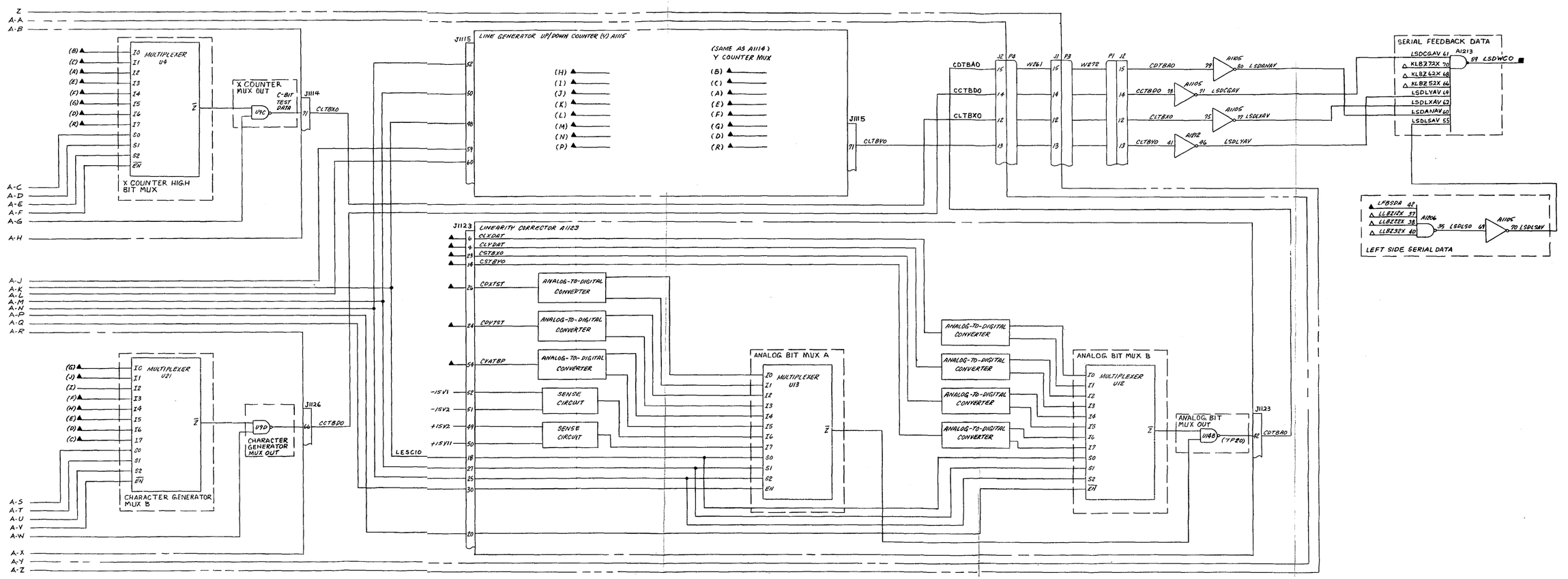
FO-52. Computer Buffer/CBIT Bit Sample Multiplexing Logic Diagram (Sheet 1 of 4)



FO-52. Computer Buffer/CBIT Bit Sample Multiplexing Logic Diagram (Sheet 2 of 4)



FO-52. Computer Buffer/CBIT bit Sample Multiplexing Logic Diagram (Sheet 3 of 4)



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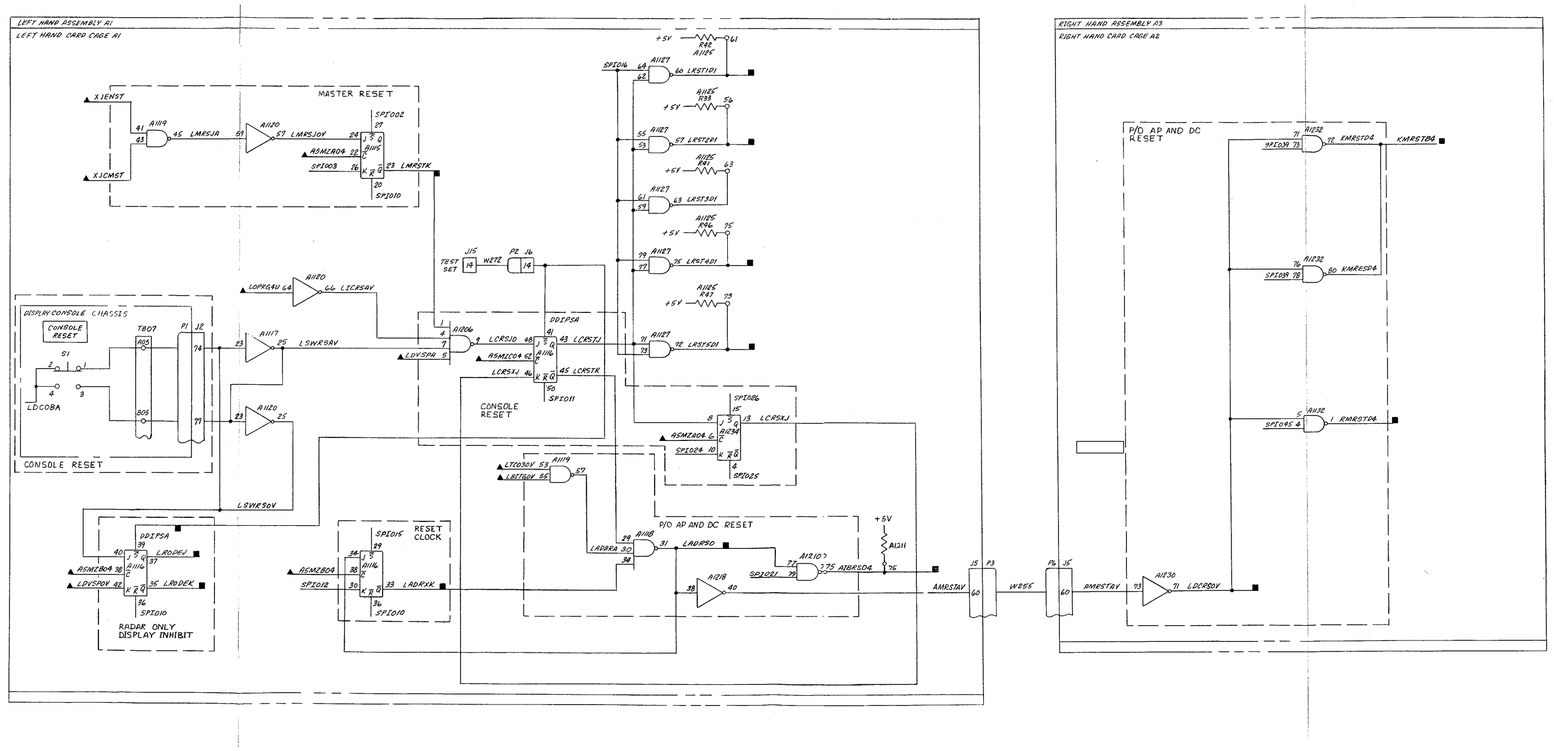
FO-52. Computer Buffer/C-BIT Bit Sample Multiplexing Logic Diagram (Sheet 4 of 4)

INPUTS	F/O - SH	INPUTS	F/O - SH
ASMZA04	54-2	LDVSP0V	50-2
ASMZB04	54-2	L0PRG4U	51-0
ASMZC04	54-2	LTC030V	49-0
LBITG0V	49-0	XJCMST	48-1
LDC0BA	50-2	XJENST	48-1
LDVSPA	50-2		

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
AIRRSD4	1-0	LADR50	1-0
	3-0		13-0
	4-0	LADRXK	49-0
	12-0	LCRSTK	48-1
	51-0		49-0
AMRSTAV	5-0		50-2
	9-1		51-0
	10-0	LDCR50V	25-2
	12-0	LMRSTK	50-2
DDIPSA	48-1	L80DEJ	8-2
KMRSTB4	19-1	L80DEK	50-2
	22-0	LRST1D1	49-0
	24-0		50-2
	28-0		52-1
	29-0	LRST2D1	49-0
	35-0		52-1
	36-1	LRST4D1	47-0
	44-1		49-0
			50-2
			51-0
		LRST5D1	50-2
			52-1
		RMRSTD4	41-1
			42-0
			45-2



FO-53. Computer Buffer/C-BIT Initialization Logic Diagram

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
2. ALL CIRCUITS SHOWN ON THIS FIGURE ARE CONTAINED ON LEFT HAND CARD CAGE A1A1. (SINCE MULTIPLE DISPLAY CONSOLES ARE USED, ABBREVIATED DESIGNATIONS ARE SHOWN).
3. DEFINITIONS FOR SYMBOLS SHOWN ARE AS FOLLOWS:

   ▲ INPUT FROM ANOTHER FIGURE
   △ INPUT FROM SAME FIGURE
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5. REFER TO TABLE 5-6 THRU 5-8 FOR COMPLETE SIGNAL LOOK UP AND CIRCUIT CARD TEST POINTS.
6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.
8. SPIXXX INDICATES +5V PULL UP THROUGH RESISTOR CARDS; REFER TO TABLE 5-6 THRU 5-8 FOR COMMON LISTING.
9. INDICATES FRONT PANEL MARKING.

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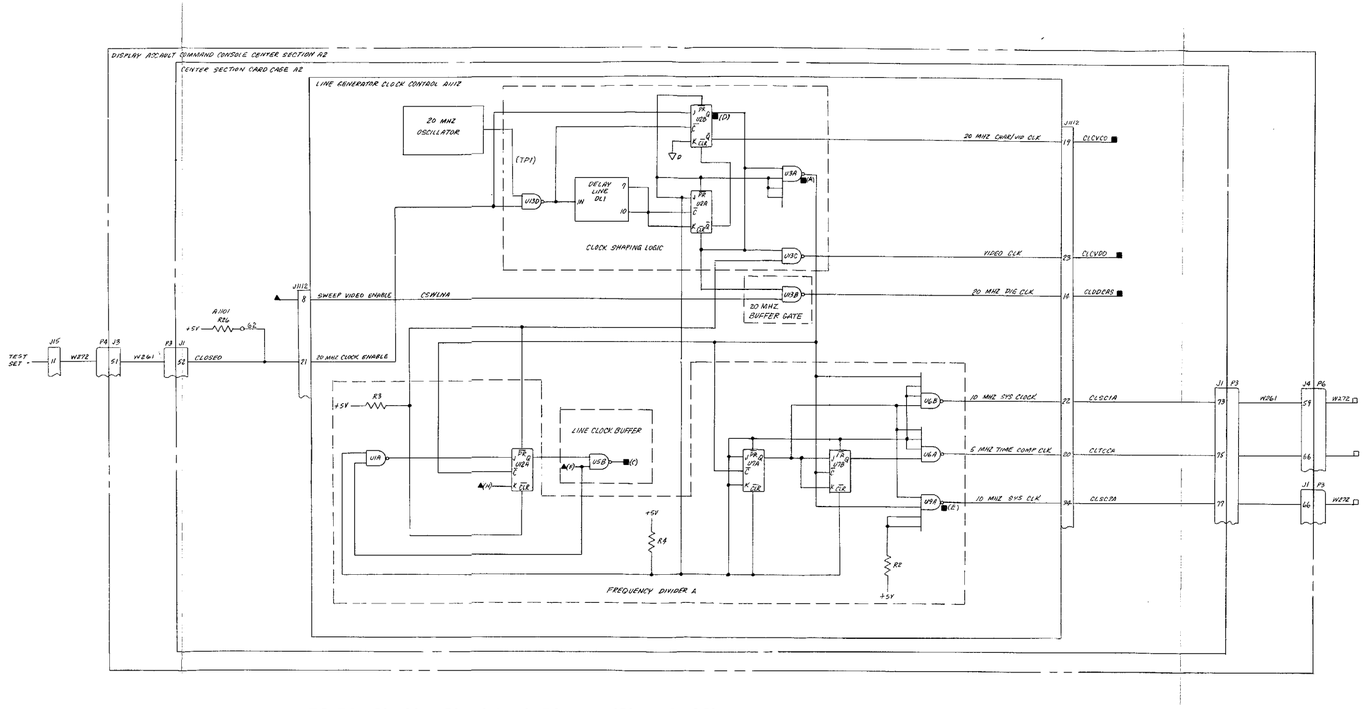
INPUTS	F/O - SH
CSWLSRA	27-2
VACENS	36-7
VBCENS	36-3
A1112(F)	27-1
A1112(H)	37-1

OUTPUTS	F/O - SH	OUTPUTS	F/O - SH	OUTPUTS	F/O - SH	OUTPUTS	F/O - SH
ACTRKA	7-1	A5MZE04	9-3	K5MZA04	22-0	K6MZRA	41-2
	9-1		11-0		36-1		41-3
	12-9		12-0		42-0		41-4
AMWRK0	2-0		48-1		45-1		44-2
	7-0		49-0		46-0	VACP60	34-2
A5MSQK	51-0		50-2	K5MZBAH	16-2	VAC5004	35-0
	54-2	A5MZE04	5-0		16-4		34-2
A5MZAA	6-1		11-0		25-2	VBC5004	36-2
	6-2		49-0		29-0	VBD5004	36-3
	6-3		50-2	K5MZBG4	24-0	VBGP60	34-3
	12-0		52-1		25-0	VCLK504	32-0
	52-1	A5SQFAV	7-2		36-1		35-0
A5MZA04	5-0	A5SQT0	4-0		41-2		36-2
	9-2	A10MA04	1-0		42-0	A1117(A)	37-1
	48-1		47-0		46-0	A1112(C)	37-1
	50-2		48-0	K5MZCAH	23-0	A1112(D)	37-1
	51-0		51-0		30-0	A1112(E)	37-1
	53-0	A10MB04	4-0	K5MZC04	22-0		
A5MZB04	9-2	A10MC04	4-0		28-0		
	11-0		51-0		36-1		
	44-2	A10MZ04	4-0		41-2		
	48-1	A10NRA	2-0		43-0		
	50-2		3-0	K5MZD0	19-2		
	52-1		51-0		22-0		
	53-0	A10NCA	2-0		23-0		
A5MZC04	4-0	CLCVC0	37-1	K5MZE04	21-0		
	9-2		38-3		22-0		
	10-0		40-1		23-1		
	48-1	CLCVD0	39-2		36-1		
	49-0	CLDOCA5	37-2		41-2		
	50-2		37-4		43-2		
	53-0	KCTRKA	17-1	K5MZC0	28-0		
			19-1		42-0		
			24-0	K5SQVAV	17-0		
		K5WFRK0	17-2	LCTRKA	41-2		
		K5MLD04	22-0		50-2		
			28-0		51-0		



FO-54. Clocking Circuit Logic Diagram (Sheet 1 of 3)

NOTES: UNLESS OTHERWISE SPECIFIED

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN ; FOR COMPLETE DESIGNATIONS , PREFIX WITH APPLICABLE UNIT NUMBER AND ASSEMBLY DESIGNATION.
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6. REFER TO DISPLAY CONSOLE POWER DISTRIBUTION DIAGRAMS FOR DC POWER AND GROUND CIRCUITS.
7. CIRCUIT SYMBOLS INCLUDE CARD LOCATIONS AND CIRCUIT CARD PIN NUMBERS.

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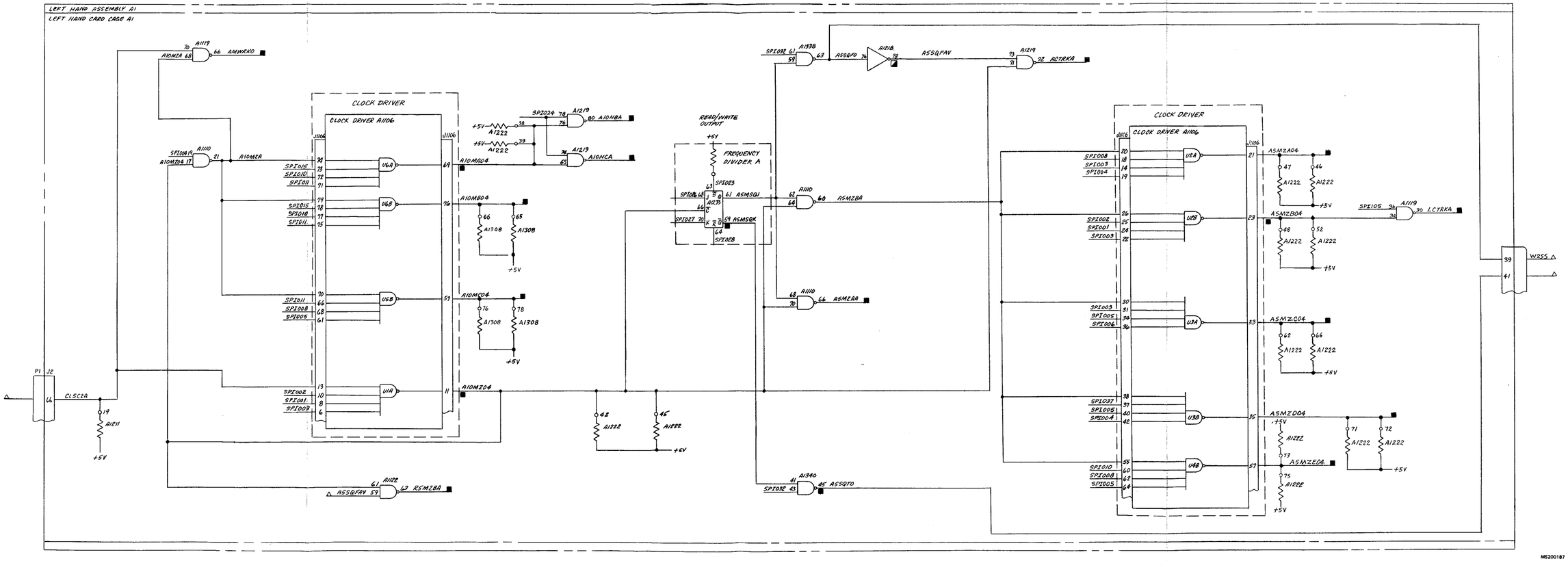
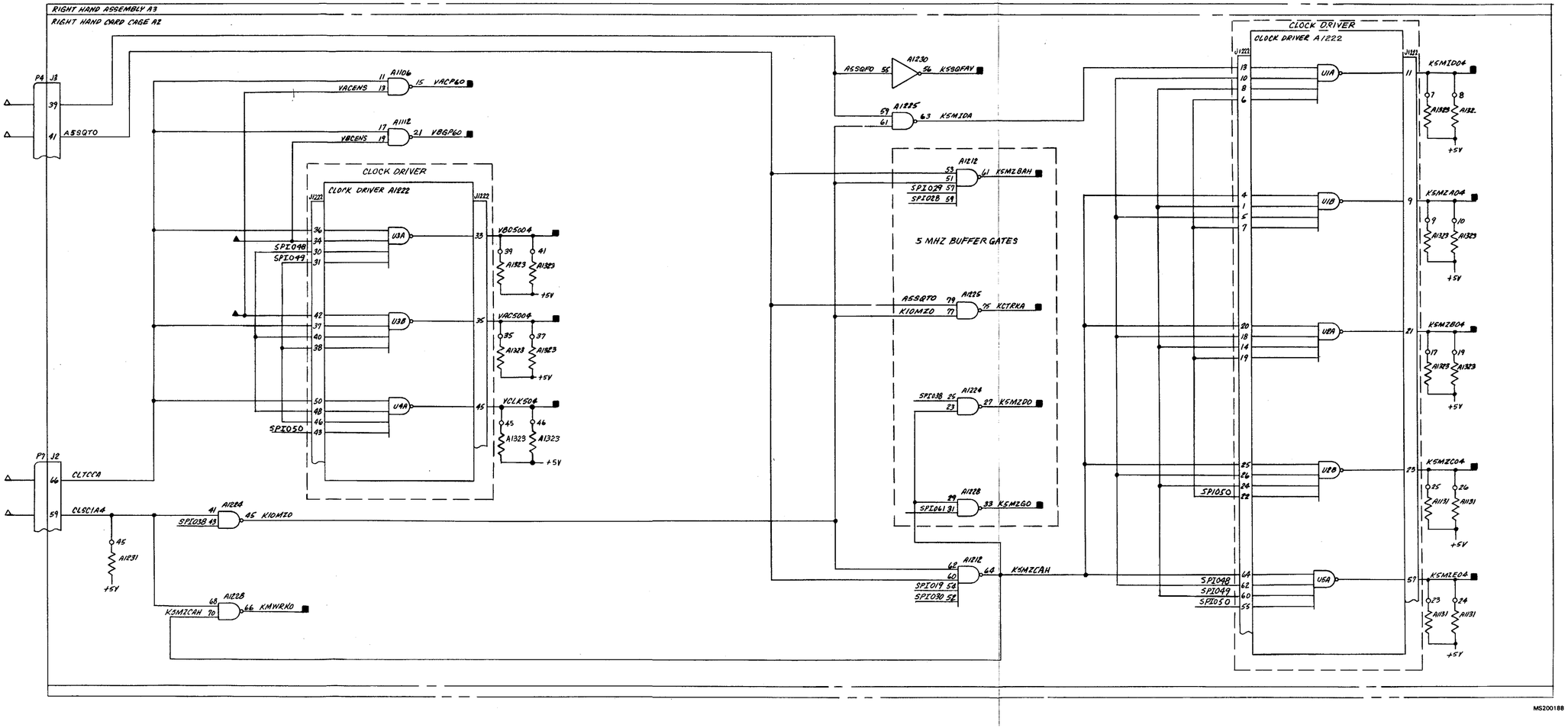


FO-54. Clocking Circuit Logic Diagram (Sheet 2 of 3)



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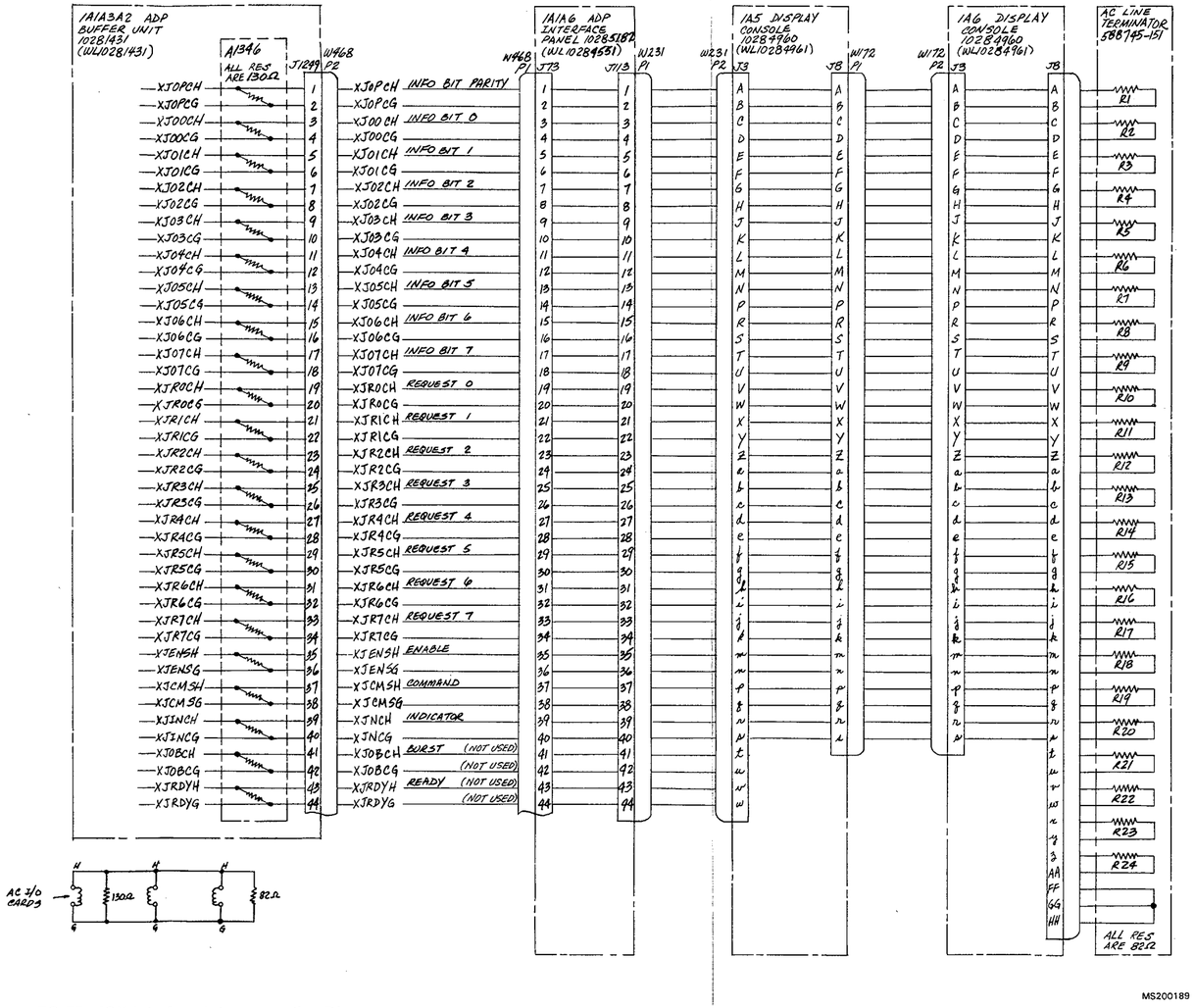
FO-54 Clocking Circuit Logic Diagram (Sheet 3 of 3)

IOX SOURCE DATA

Signal	Location	Pin	TP
XJOPCH	A1345	38	TP6B
XJOPCG	A1345	40	TP7B
XJO0CH	A1341	38	TP6B
XJO0CG	A1341	40	TP7B
XJO1CH	A1341	34	TP12B
XJO1CG	A1341	36	TP13B
XJO2CH	A1342	38	TP6B
XJO2CG	A1342	40	TP7B
XJO3CH	A1342	34	TP12B
XJO3CG	A1342	36	TP13B
XJO4CH	A1343	38	TP6B
XJO4CG	A1343	40	TP7B
XJO5CH	A1343	34	TP12B
XJO5CG	A1343	36	TP13B
XJO6CH	A1344	38	TP6B
XJO6CG	A1344	40	TP7B
XJO7CH	A1344	34	TP12B
XJO7CG	A1344	36	TP13B
XJR0CH	A1335	38	TP6B
XJR0CG	A1335	40	TP7B
XJR1CH	A1335	34	TP12B
XJR1CG	A1335	36	TP13B
XJR2CH	A1336	38	TP6B
XJR2CG	A1336	40	TP7B
XJR3CH	A1336	34	TP12B
XJR3CG	A1336	36	TP13B
XJR4CH	A1337	38	TP6B
XJR4CG	A1337	40	TP7B
XJR5CH	A1337	34	TP12B
XJR5CG	A1337	36	TP13B
XJR6CH	A1338	38	TP6B
XJR6CG	A1338	40	TP7B
XJR7CH	A1338	34	TP12B
XJR7CG	A1338	36	TP13B
XJENSH	A1340	34	TP12B
XJENSG	A1340	36	TP13B
XJCMSH	A1340	38	TP6B
XJCMSG	A1340	40	TP7B
XJINCH	A1345	34	TP12B
XJINCG	A1345	36	TP13B
XJOBCH	A1339	38	TP6B
XJOBCG	A1339	40	TP7B
XJRDYH	A1339	34	TP12B
XJRDYG	A1339	36	TP13B



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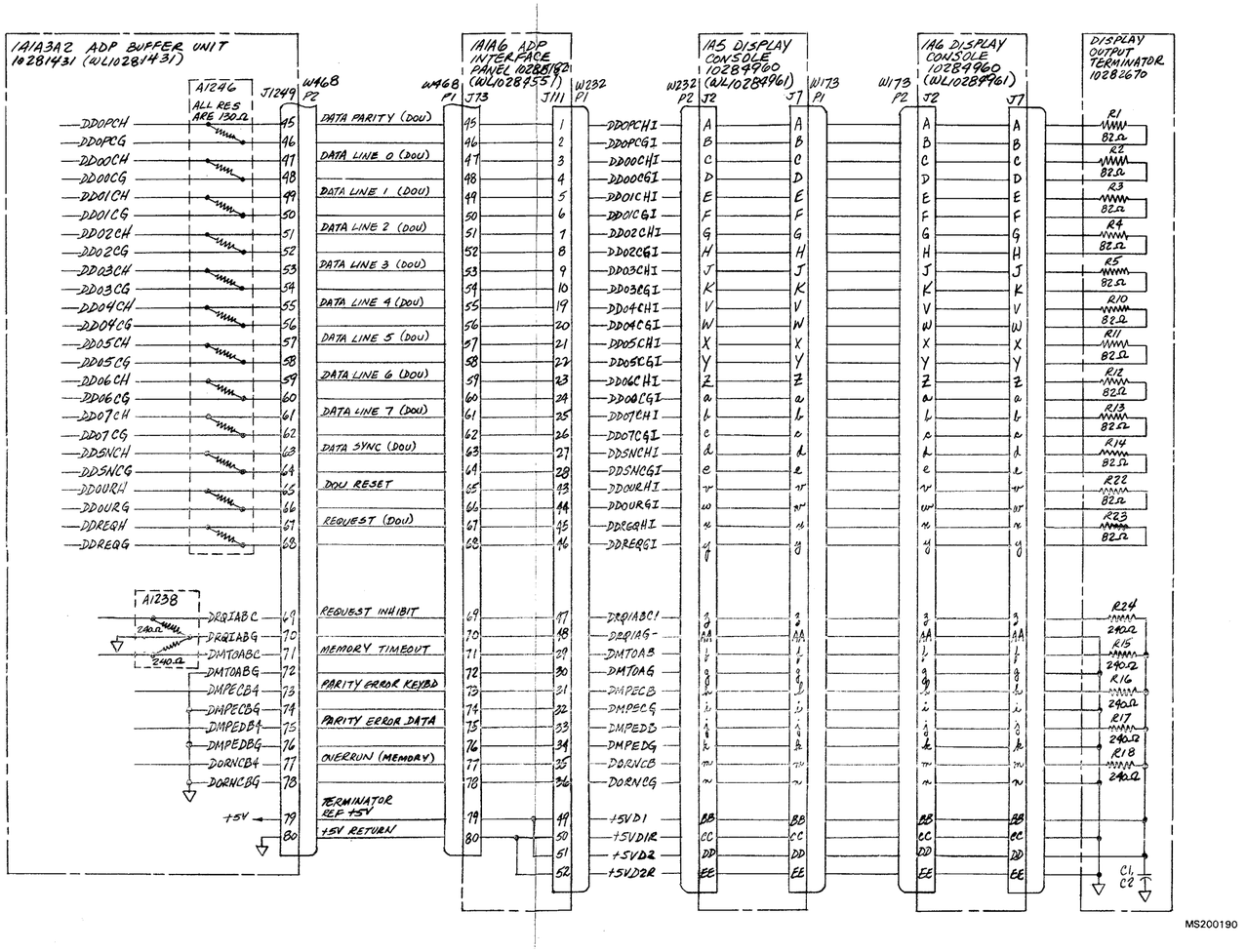
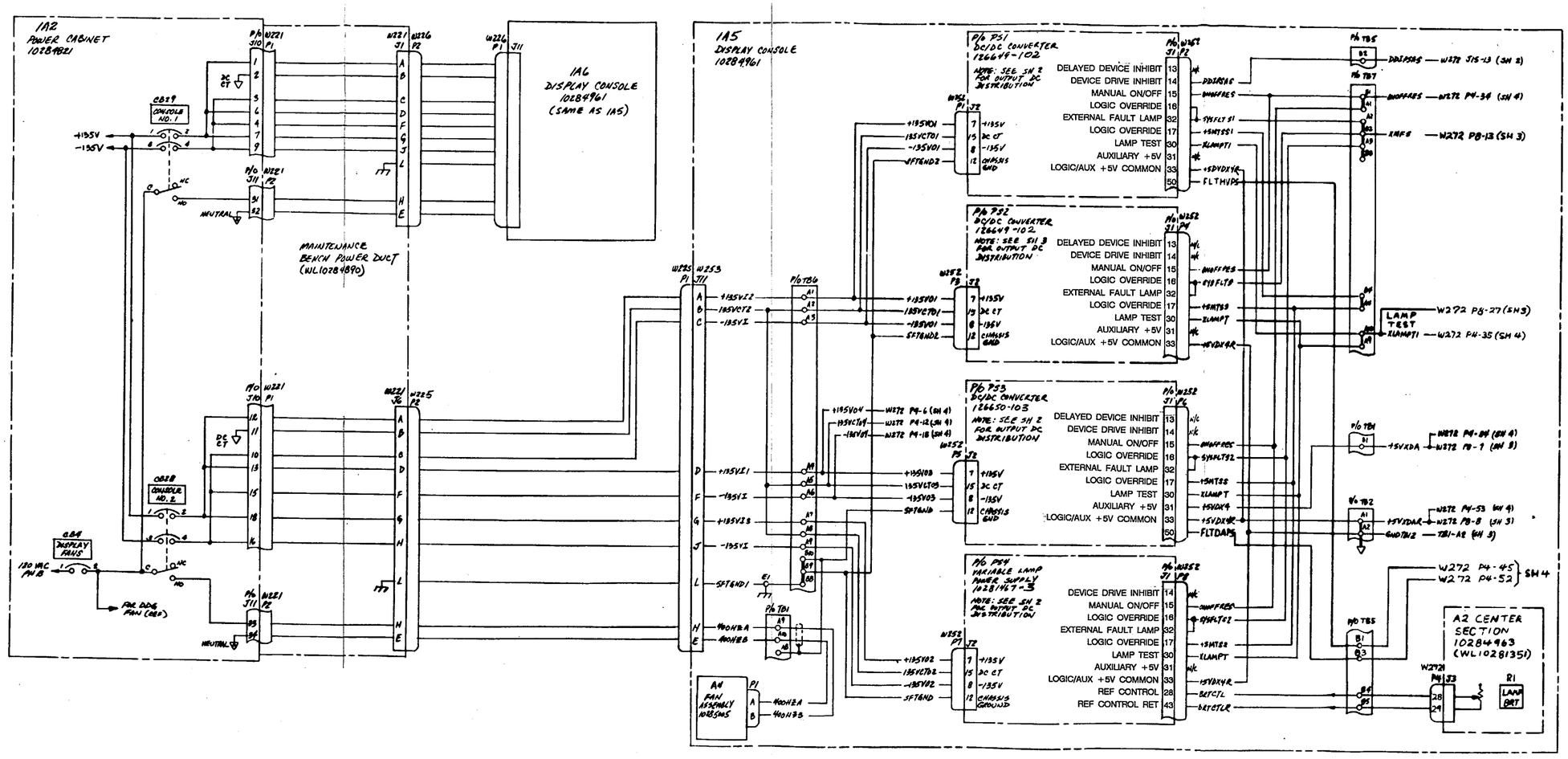
FO-55. IOX Interface Interconnection Diagram

DOU SOURCE DATA

Signal	Location	Pin	TP
DDOPCH	A1241	34	TP12B
DDOPCG	A1241	36	TP13B
DDO0CH	A1242	38	TP6B
DDO0CG	A1242	40	TP7B
DDO1CH	A1242	34	TP12B
DDO1CG	A1242	36	TP13B
DDO2CH	A1243	38	TP6B
DDO2CG	A1243	40	TP7B
DDO3CH	A1243	34	TP12B
DDO3CG	A1243	36	TP13B
DDO4CH	A1244	38	TP6B
DDO4CG	A1244	40	TP7B
DDO5CH	A1244	34	TP12B
DDO5CG	A1244	36	TP13B
DDO6CH	A1245	38	TP6B
DDO6CG	A1245	40	TP7B
DDO7CH	A1245	34	TP12B
DDO7CG	A1245	36	TP13B
DDSNCH	A1241	38	TP6B
DDSNCG	A1241	40	TP7B
DDOURH	A1240	34	TP12B
DDOURG	A1240	36	TP13B
DDREQH	A1240	38	TP6B
DDREQG	A1240	40	TP7B
DRQIABC	A1229	52	TP20A
DMTOABC	A1229	21	TP26A
DMPECB4	A1228	30	TP15A
DMPEDB4	A1228	21	TP10B
DORNCB4	A1228	1	TP2B



FO-56. DOU Interface Interconnection Diagram



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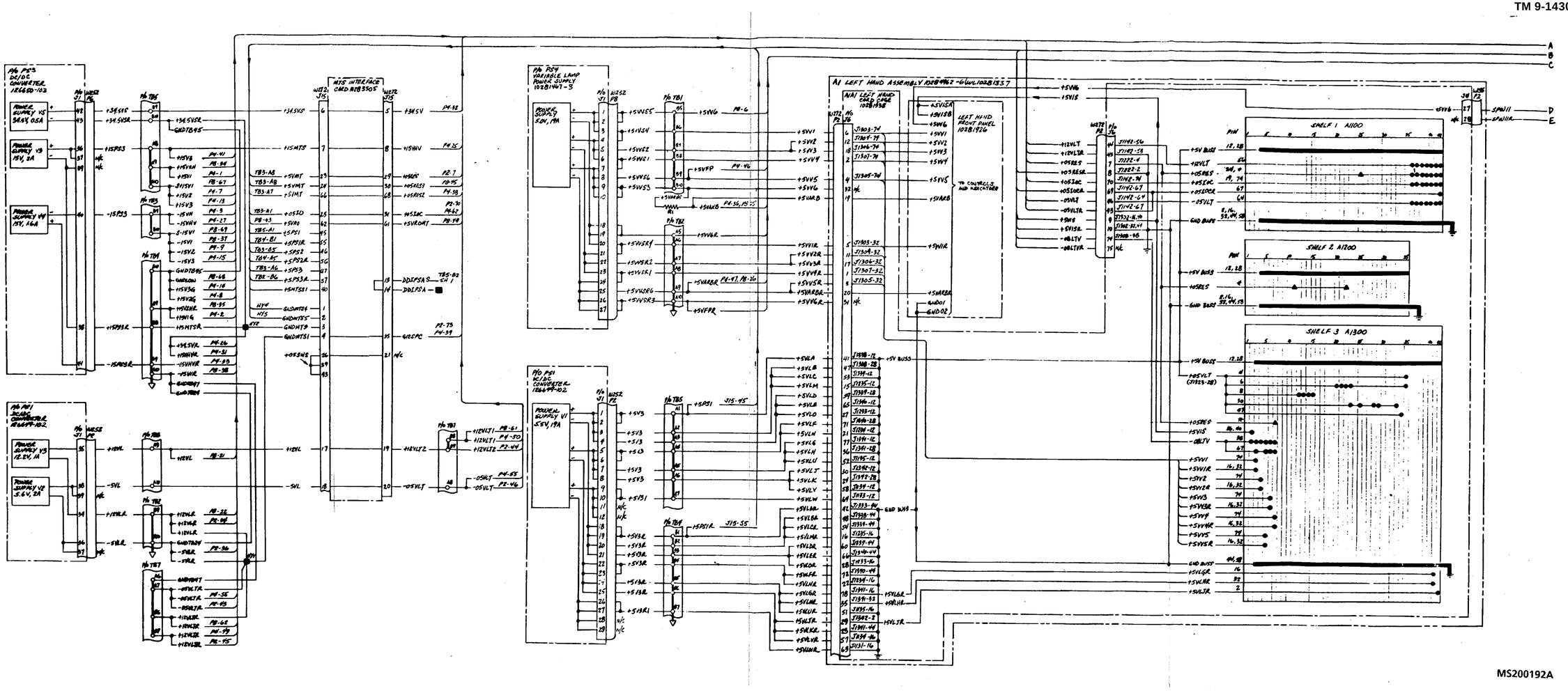
Change 1 FO-57. Display Console Power Distribution Diagram (Sheet 1 of 5)


A1 LEFT HAND ASSEMBLY 10281967-6WL10281357
A1A1 LEFT HAND CABLE ASSEMBLY 10281958
LEFT HAND FRONT PANEL 10281926
TO CONTROLS AND INDICATORS
W1T2 P2
W1T2 P6
W1T2 P8
W1T2 P16
W1T2 P4
W1T2 P12
W1T2 P14
W1T2 P10
W1T2 P18
W1T2 P20
W1T2 P22
W1T2 P24
W1T2 P26
W1T2 P28
W1T2 P30
W1T2 P32
W1T2 P34
W1T2 P36
W1T2 P38
W1T2 P40
W1T2 P42
W1T2 P44
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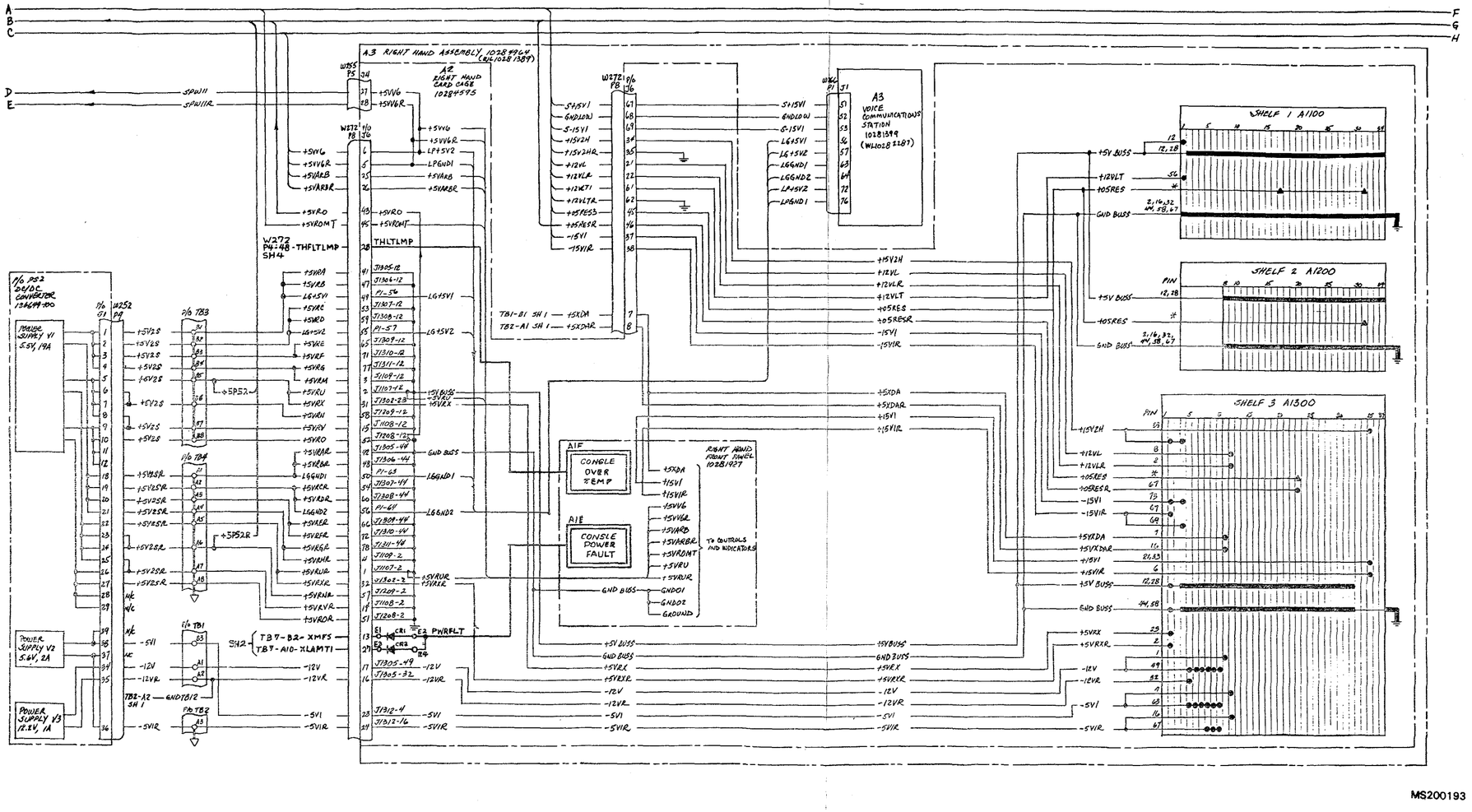
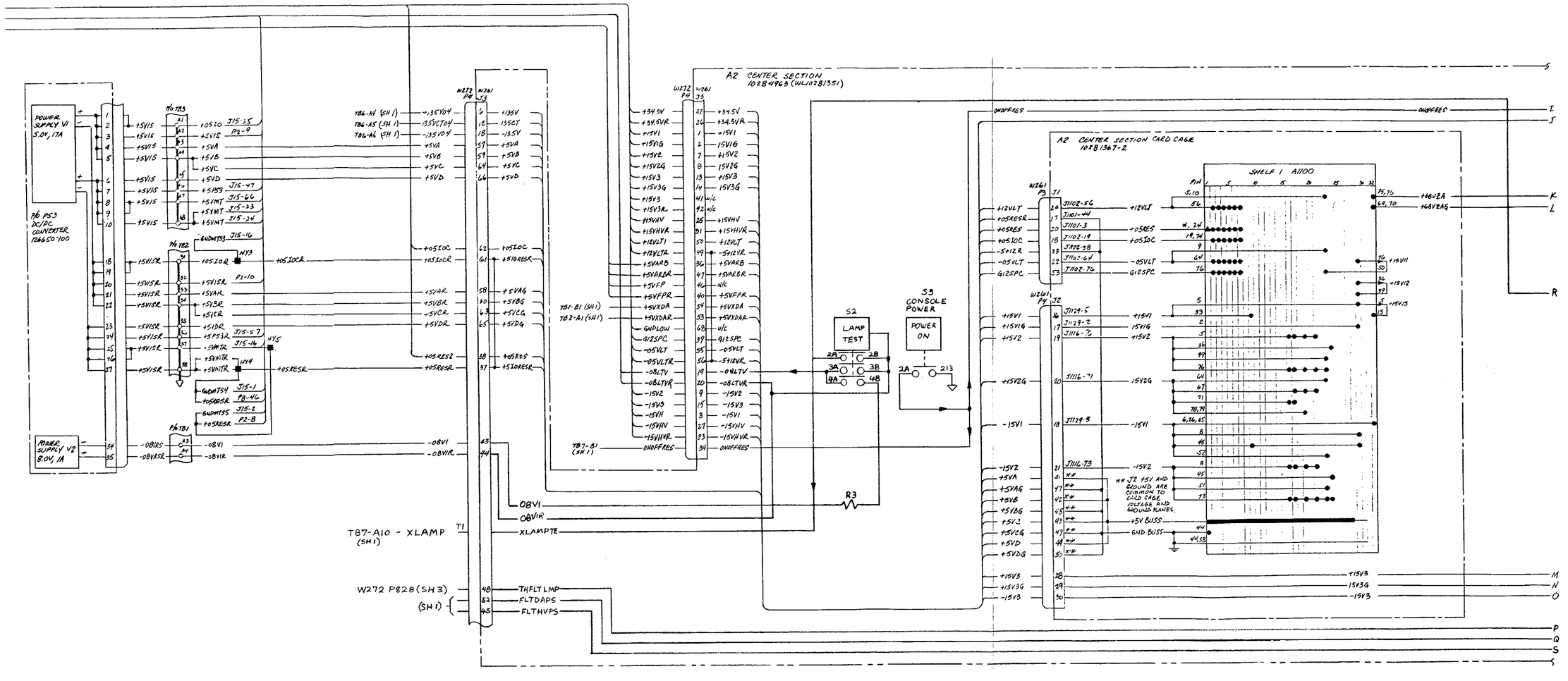
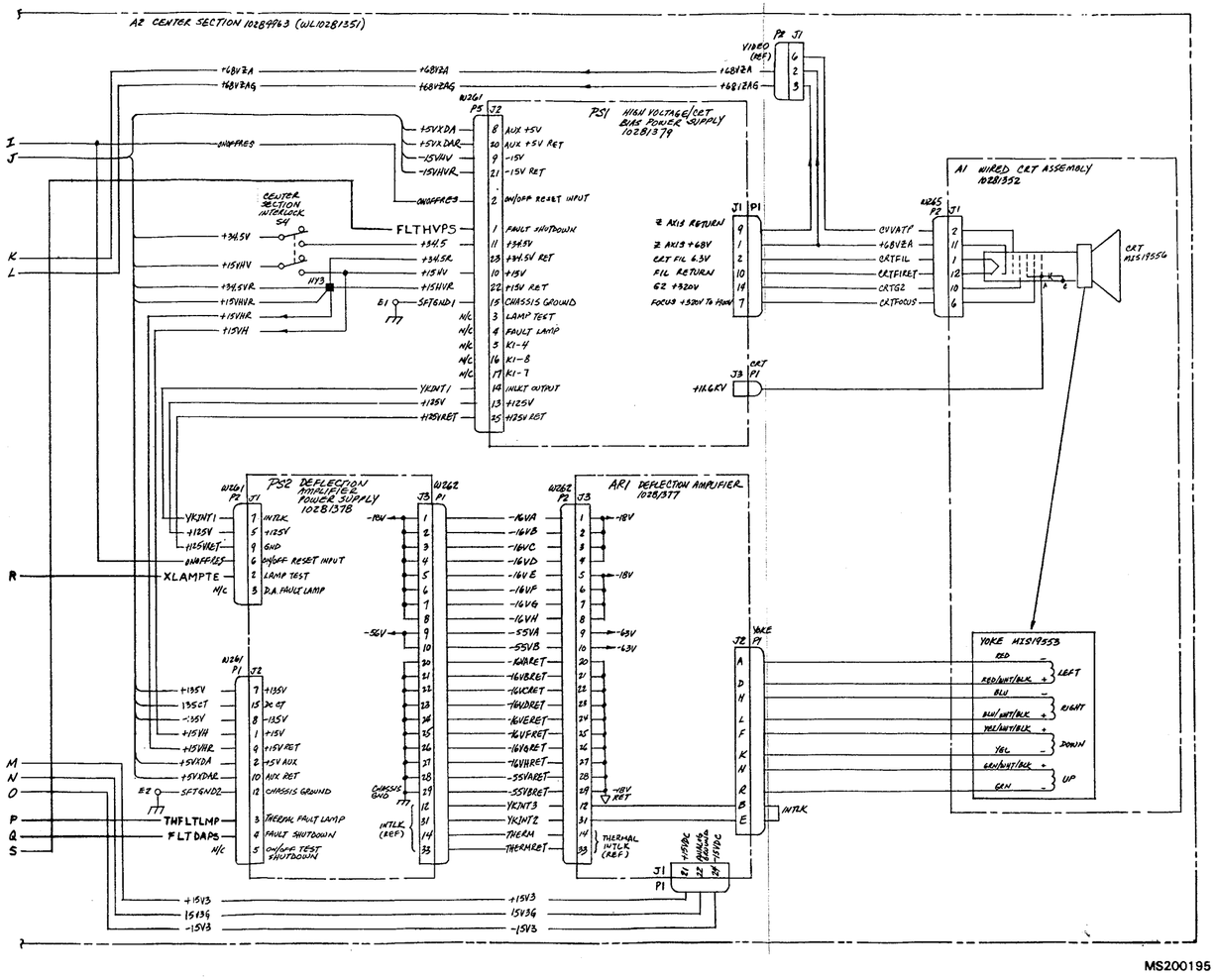
W1T2 P50
W1T2 P52
W1T2 P54
W1T2 P56
W1T2



FO-57. Display Console Power Distribution Diagram (Sheet 3 of 5)



FO-57. Display Console Power Distribution Diagram (Sheet 4 of 5)



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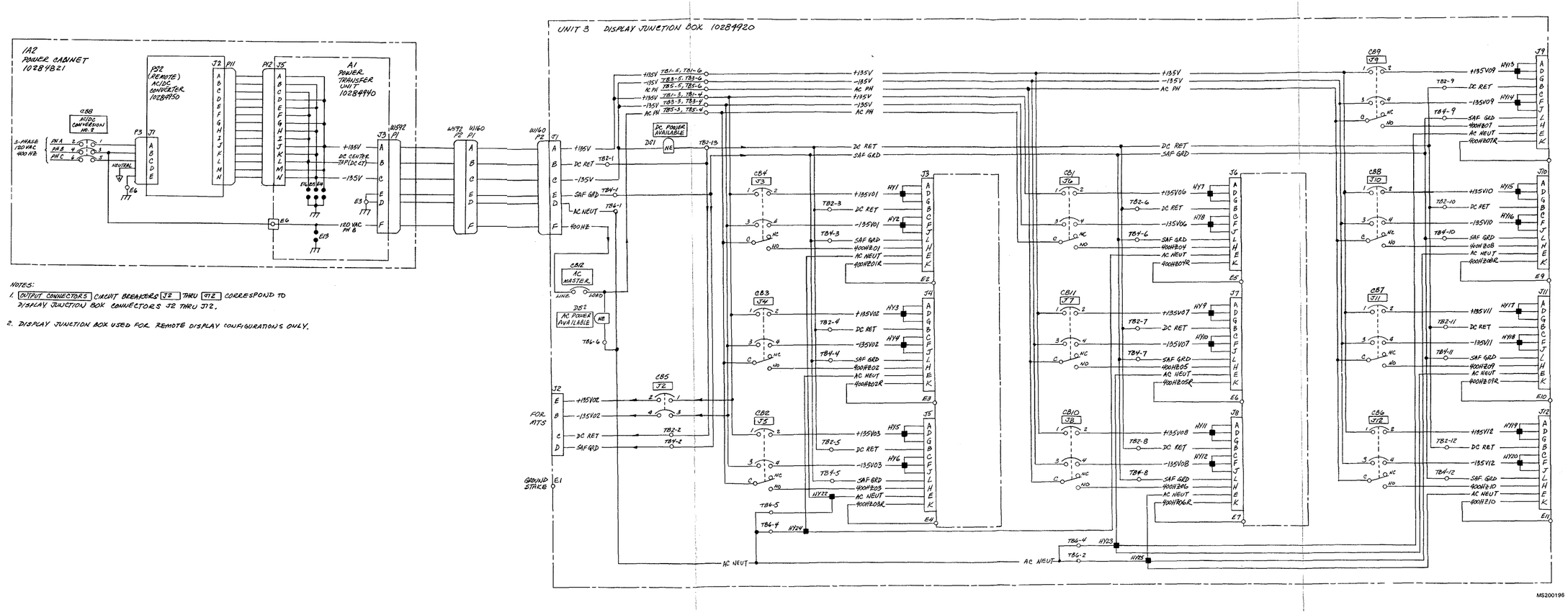
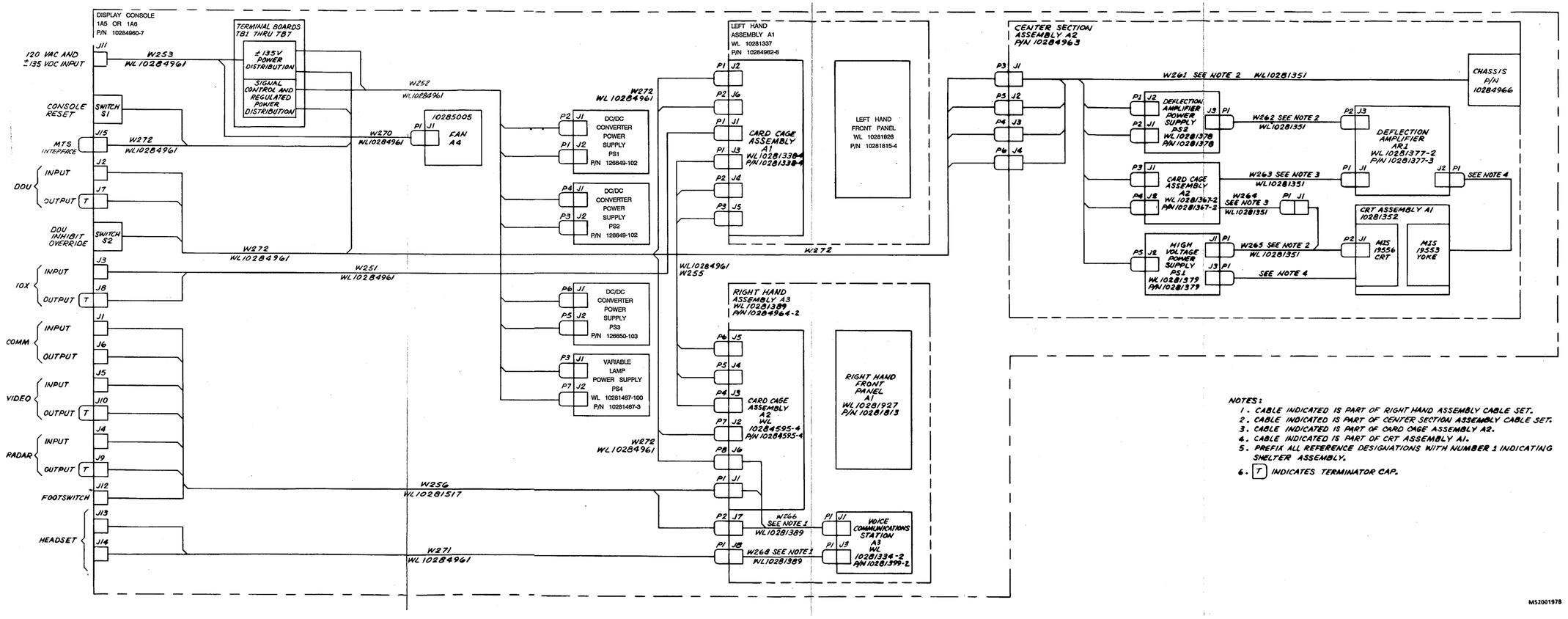
FO-57. Display Console Power Distribution Diagram (Sheet 5 of 5)



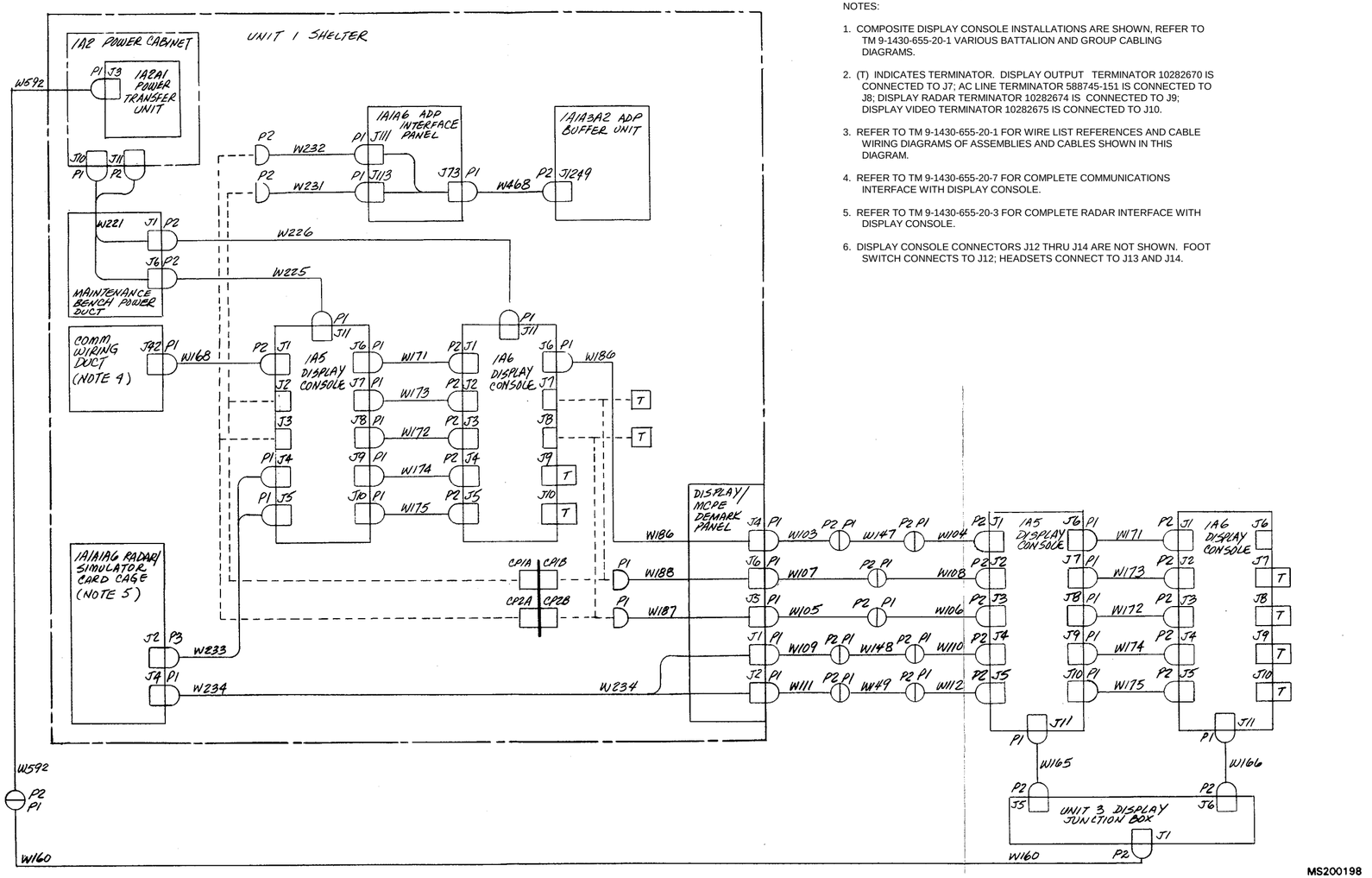
NOTES:

1. OUTPUT CONNECTORS CIRCUIT BREAKERS J2 THRU J12 CORRESPOND TO DISPLAY JUNCTION BOX CONNECTORS J2 THRU J12.
2. DISPLAY JUNCTION BOX USED FOR REMOTE DISPLAY CONFIGURATIONS ONLY.

FO-58. Remote Display Console Power Distribution Diagram)



Change 1 FO-59. Display Console Cabling Diagram

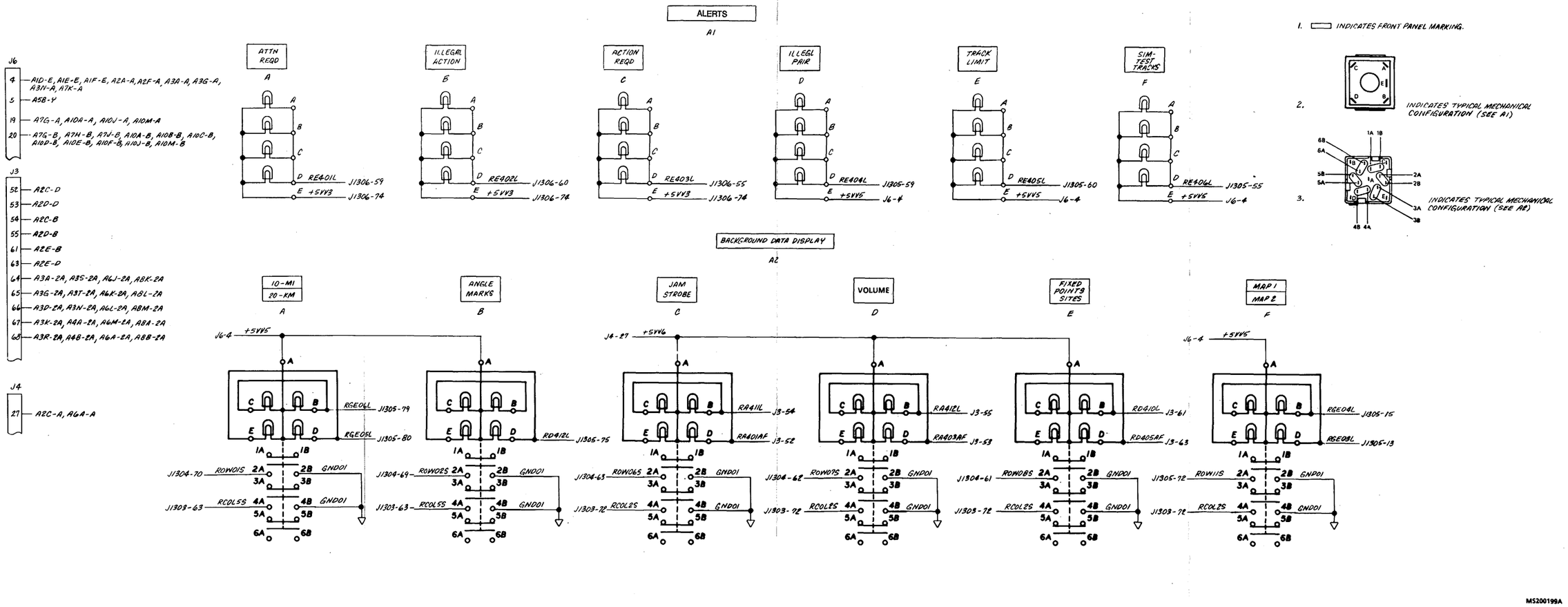


NOTES:

1. COMPOSITE DISPLAY CONSOLE INSTALLATIONS ARE SHOWN, REFER TO TM 9-1430-655-20-1 VARIOUS BATTALION AND GROUP CABLING DIAGRAMS.
2. (T) INDICATES TERMINATOR. DISPLAY OUTPUT TERMINATOR 10282670 IS CONNECTED TO J7; AC LINE TERMINATOR 588745-151 IS CONNECTED TO J8; DISPLAY RADAR TERMINATOR 10282674 IS CONNECTED TO J9; DISPLAY VIDEO TERMINATOR 10282675 IS CONNECTED TO J10.
3. REFER TO TM 9-1430-655-20-1 FOR WIRE LIST REFERENCES AND CABLE WIRING DIAGRAMS OF ASSEMBLIES AND CABLES SHOWN IN THIS DIAGRAM.
4. REFER TO TM 9-1430-655-20-7 FOR COMPLETE COMMUNICATIONS INTERFACE WITH DISPLAY CONSOLE.
5. REFER TO TM 9-1430-655-20-3 FOR COMPLETE RADAR INTERFACE WITH DISPLAY CONSOLE.
6. DISPLAY CONSOLE CONNECTORS J12 THRU J14 ARE NOT SHOWN. FOOT SWITCH CONNECTS TO J12; HEADSETS CONNECT TO J13 AND J14.

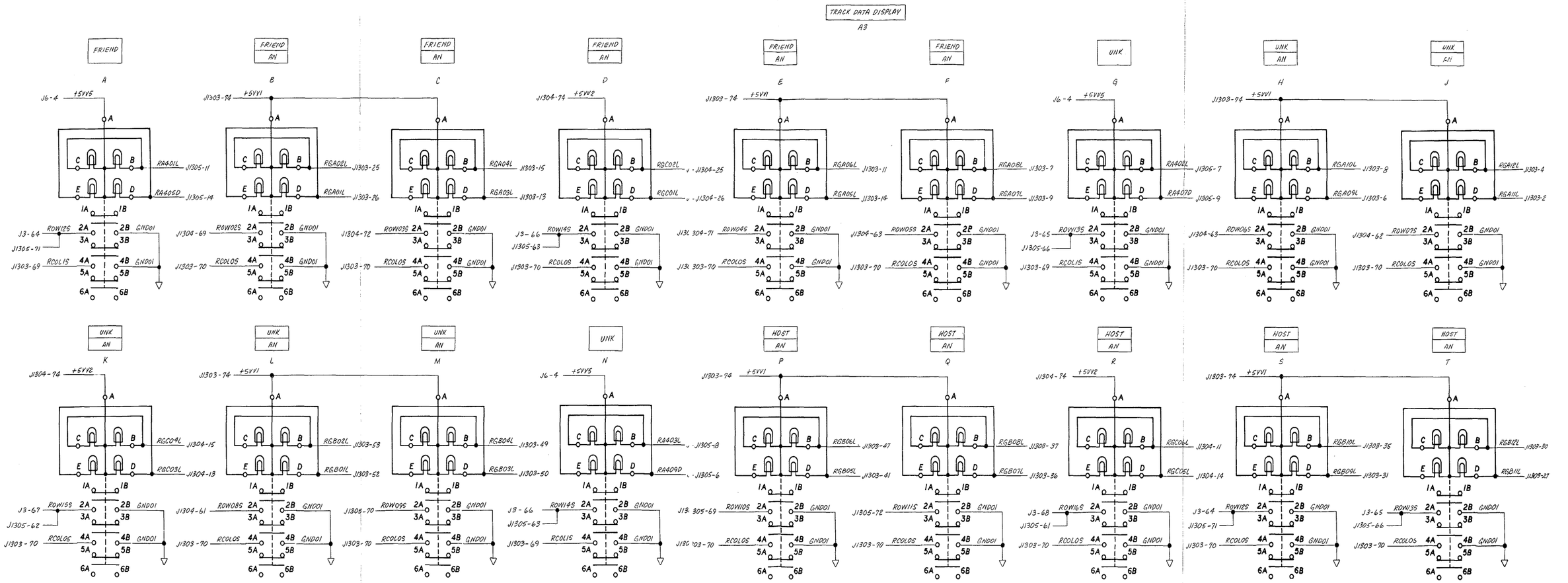
MS200198

FO-60. Display Console Interconnecting Cabling Diagram

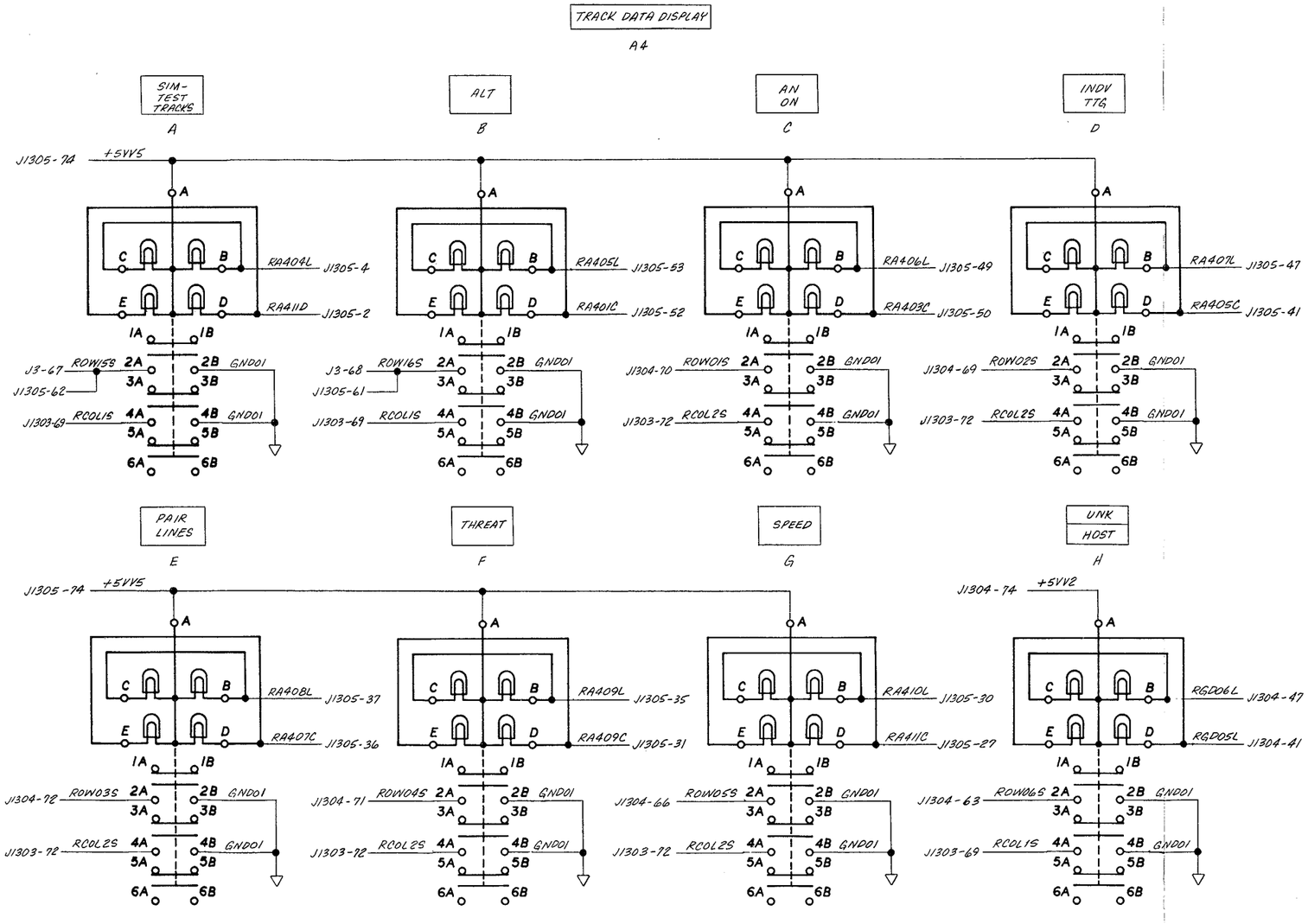


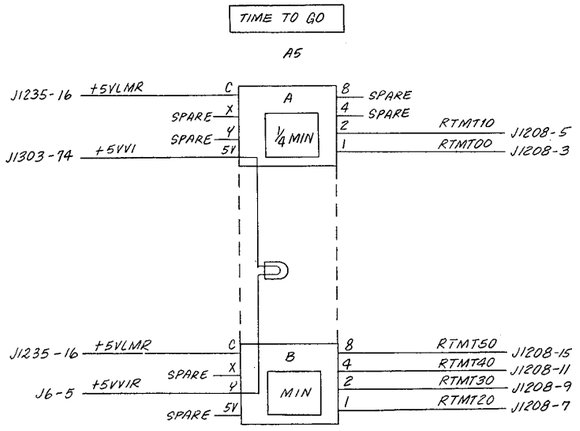
MS200199A

Change 1 FO-61. Left Hand Front Panel, Schematic Diagram (Sheet 1 of 7)

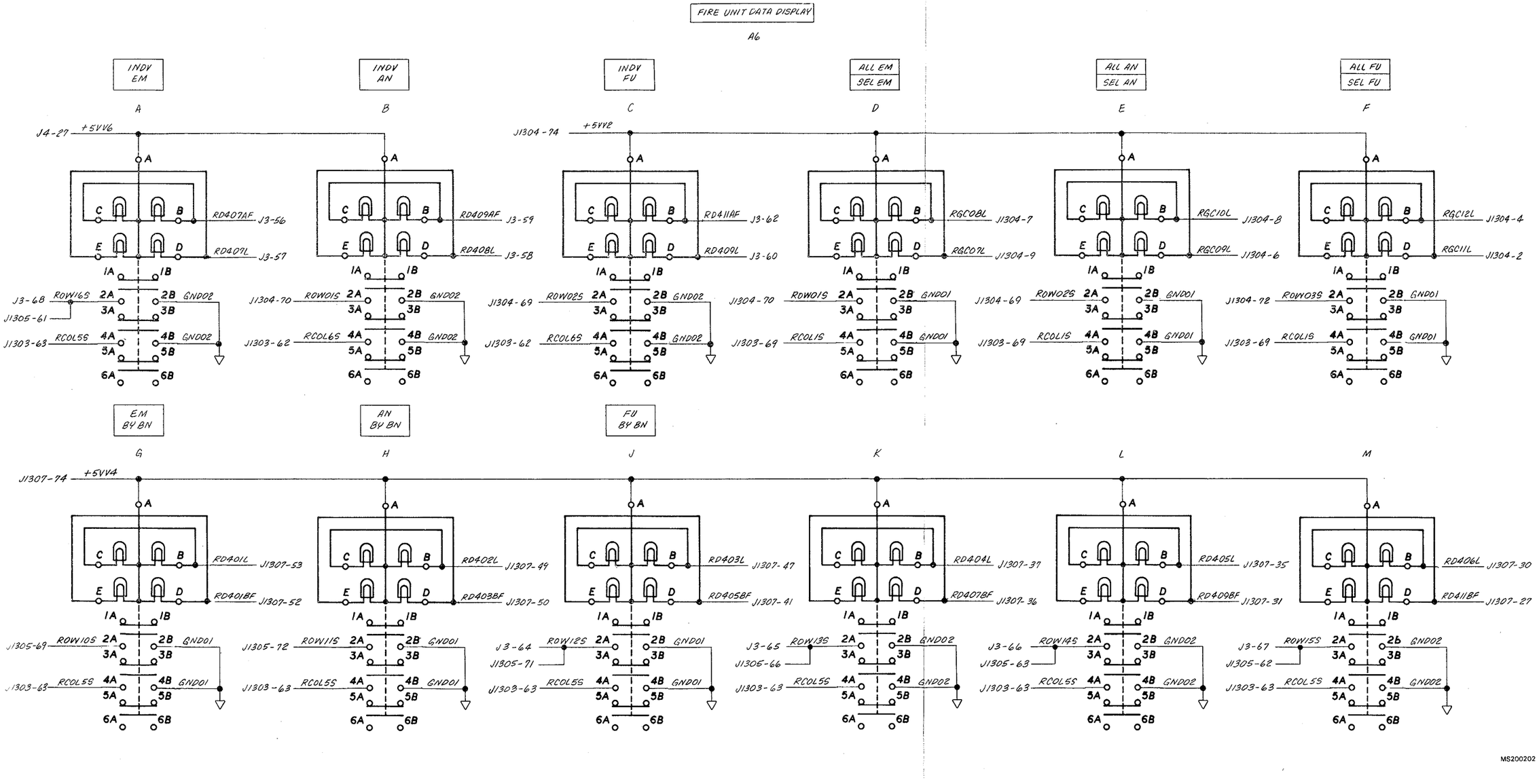


FO-61. Left Hand Front Panel, Schematic Diagram (Sheet 2 of 7)

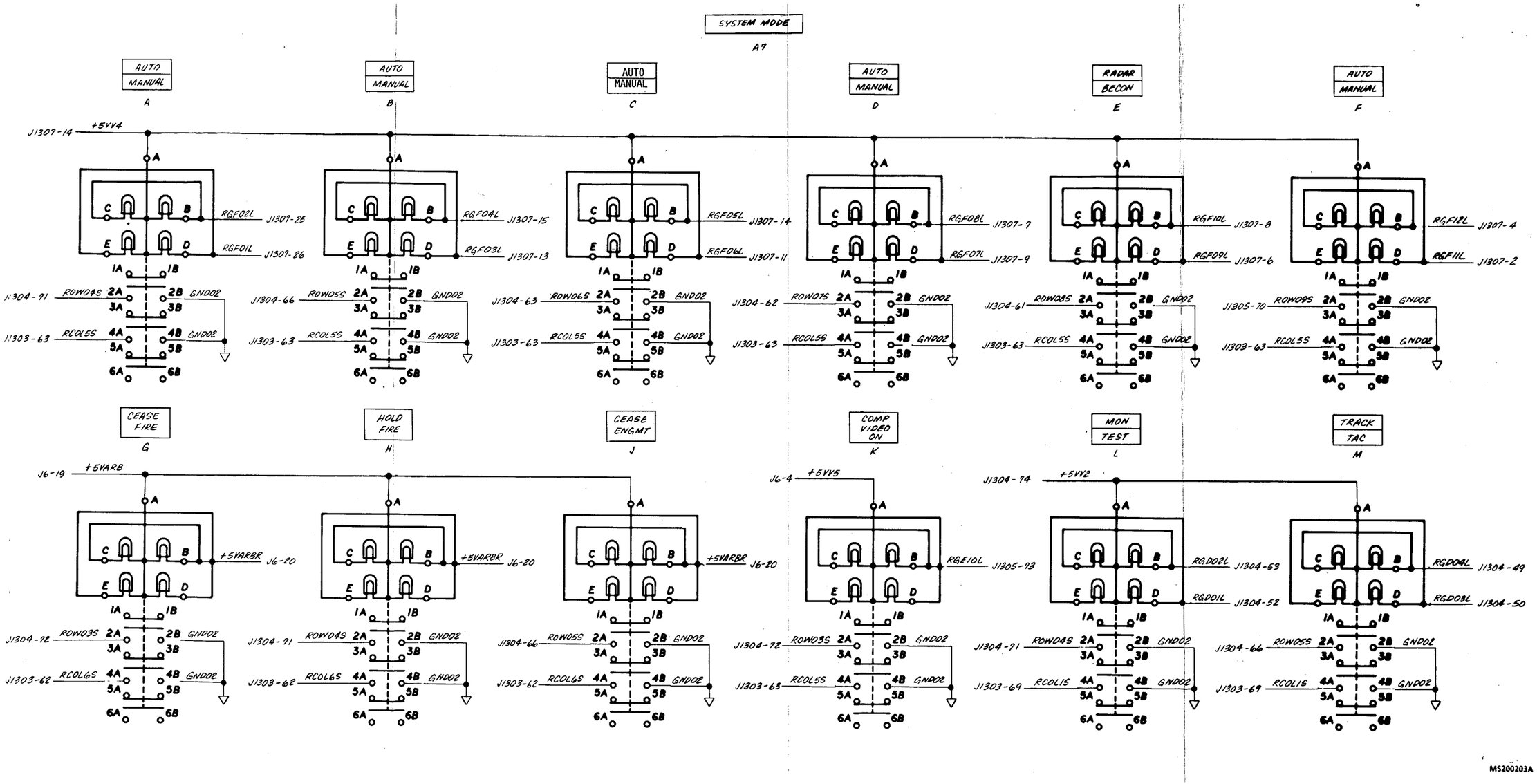




FO-61. Left Hand Front Panel, Schematic Diagram (Sheet 3 of 7)



FO-61. Left Hand Front Panel, Schematic Diagram (Sheet 4 of 7)



FO-61. Left Hand Front Panel, Schematic Diagram (Sheet 5 of 7)

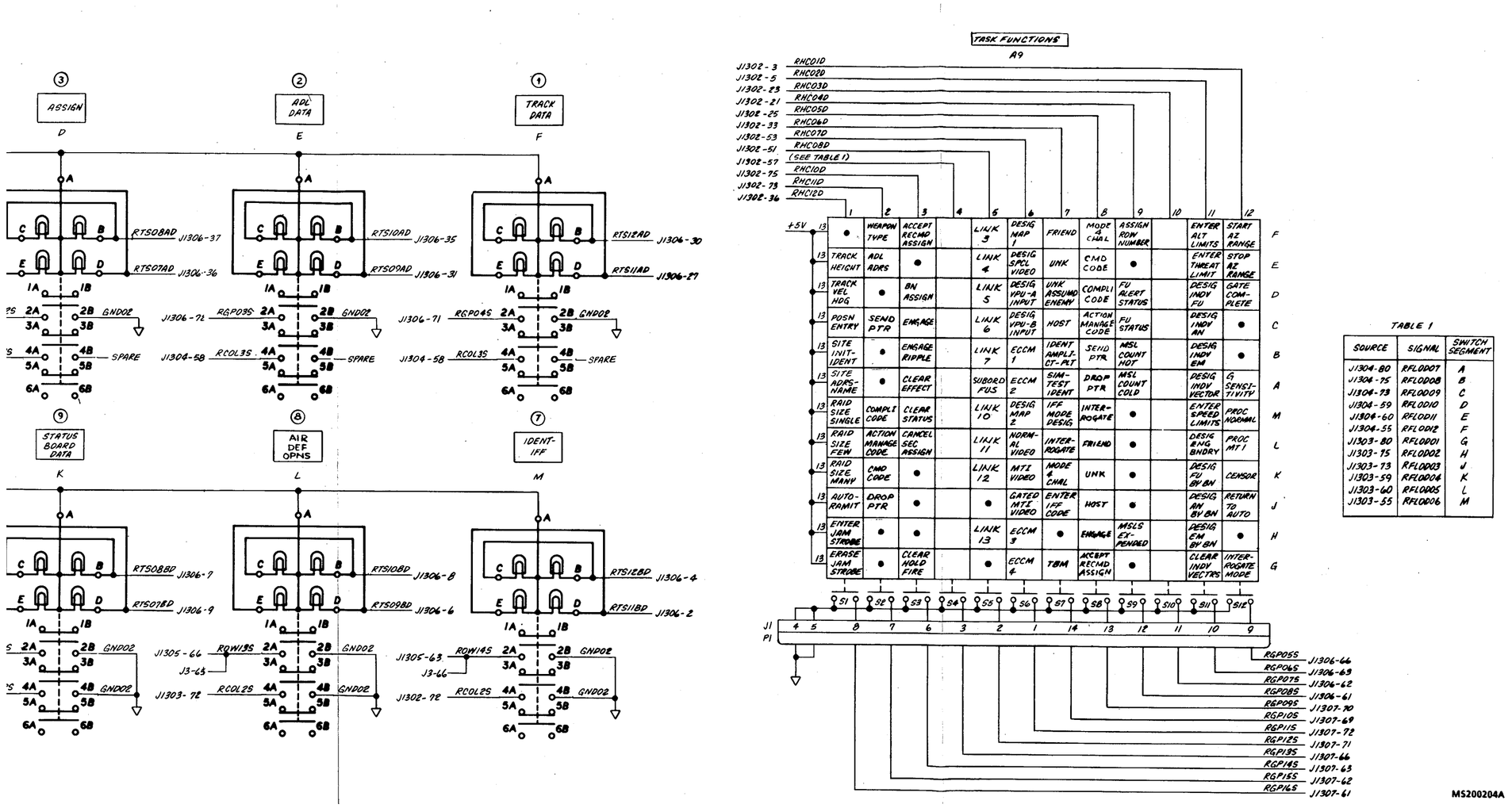
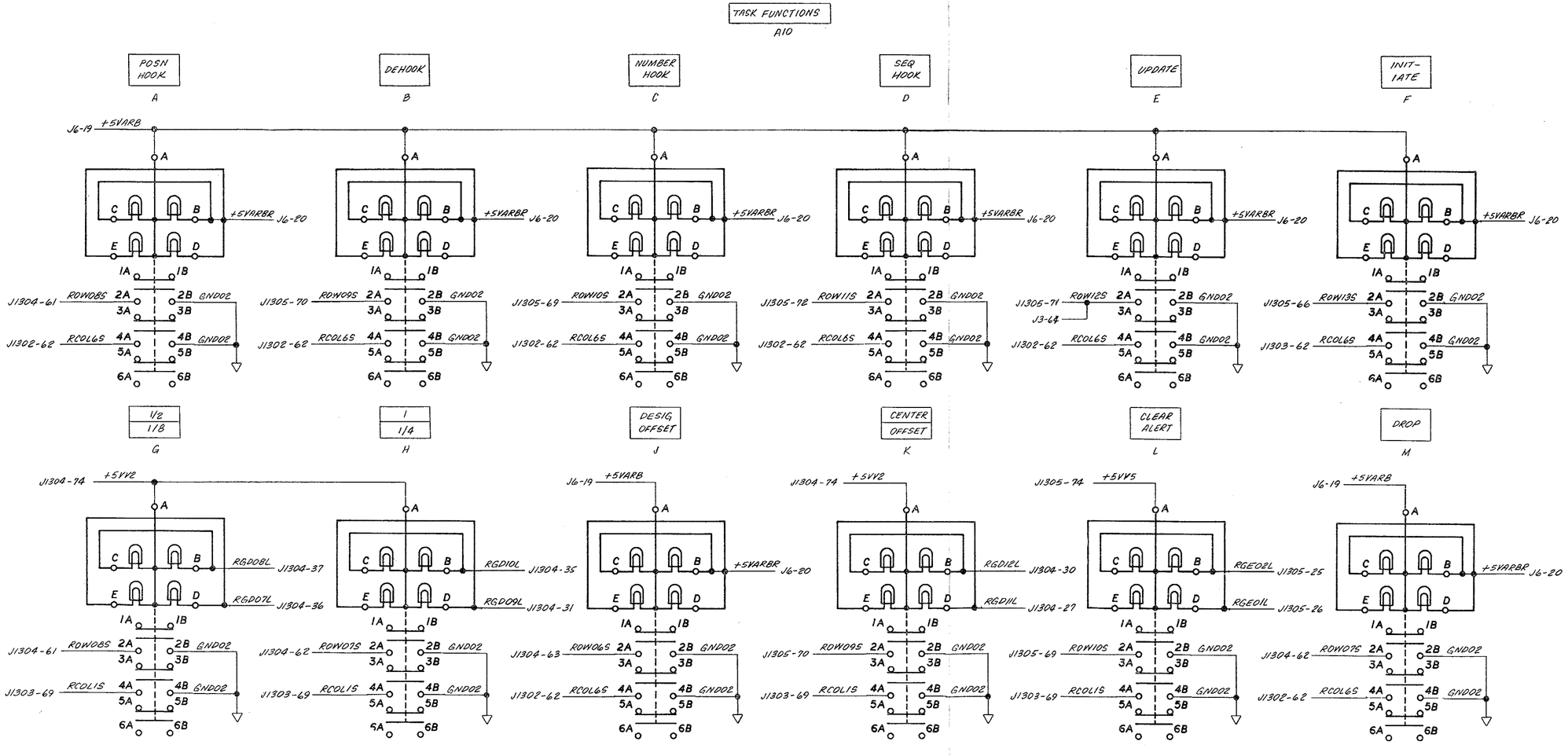


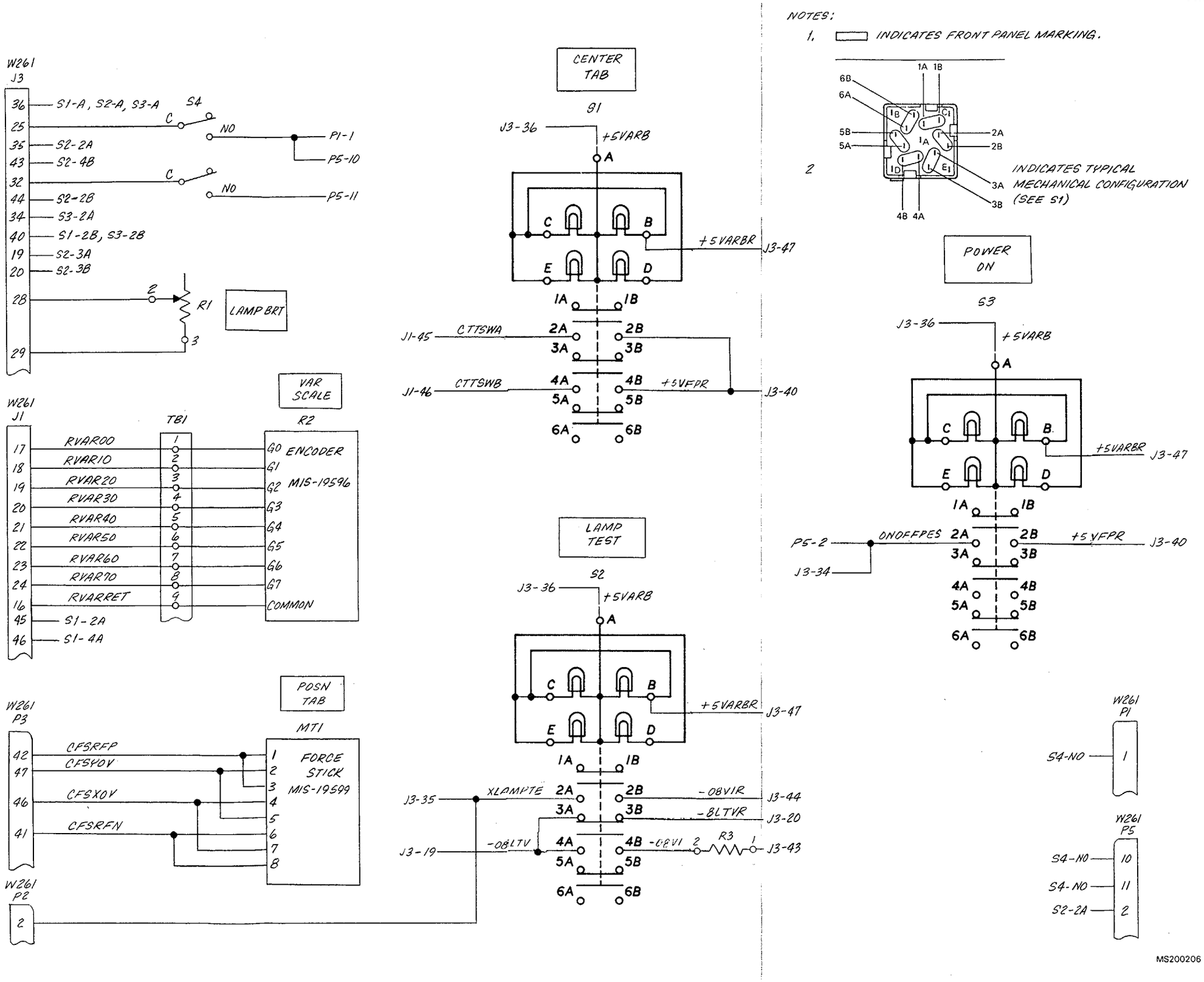
TABLE 1

SOURCE	SIGNAL	SWITCH SEGMENT
J1304-80	RFLOD07	A
J1304-75	RFLOD08	B
J1304-73	RFLOD09	C
J1304-59	RFLOD10	D
J1304-60	RFLOD11	E
J1304-55	RFLOD12	F
J1303-80	RFLOD01	G
J1303-75	RFLOD02	H
J1303-73	RFLOD03	J
J1303-59	RFLOD04	K
J1303-60	RFLOD05	L
J1303-55	RFLOD06	M

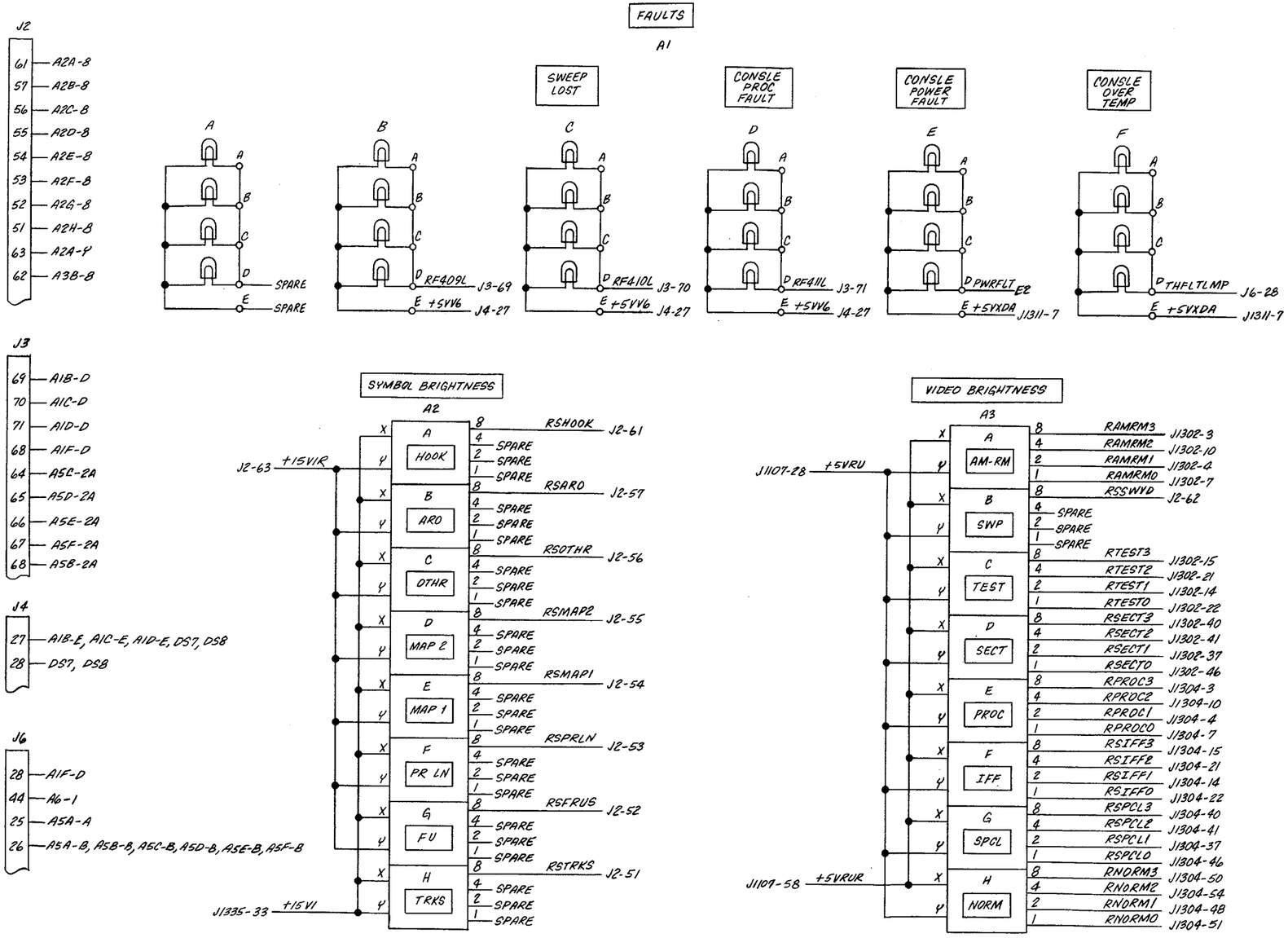
Change 1 FO-61. Left Hand Front Panel, Schematic Diagram
(Sheet 6 of 7)



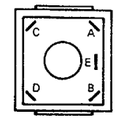
FO-61. Left Hand Front Panel, Schematic Diagram
(Sheet 7 of 7)

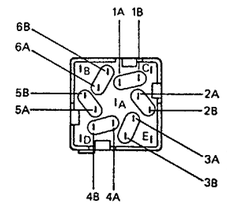


FO-62. Center Section Front Panel, Schematic Diagram



NOTES:

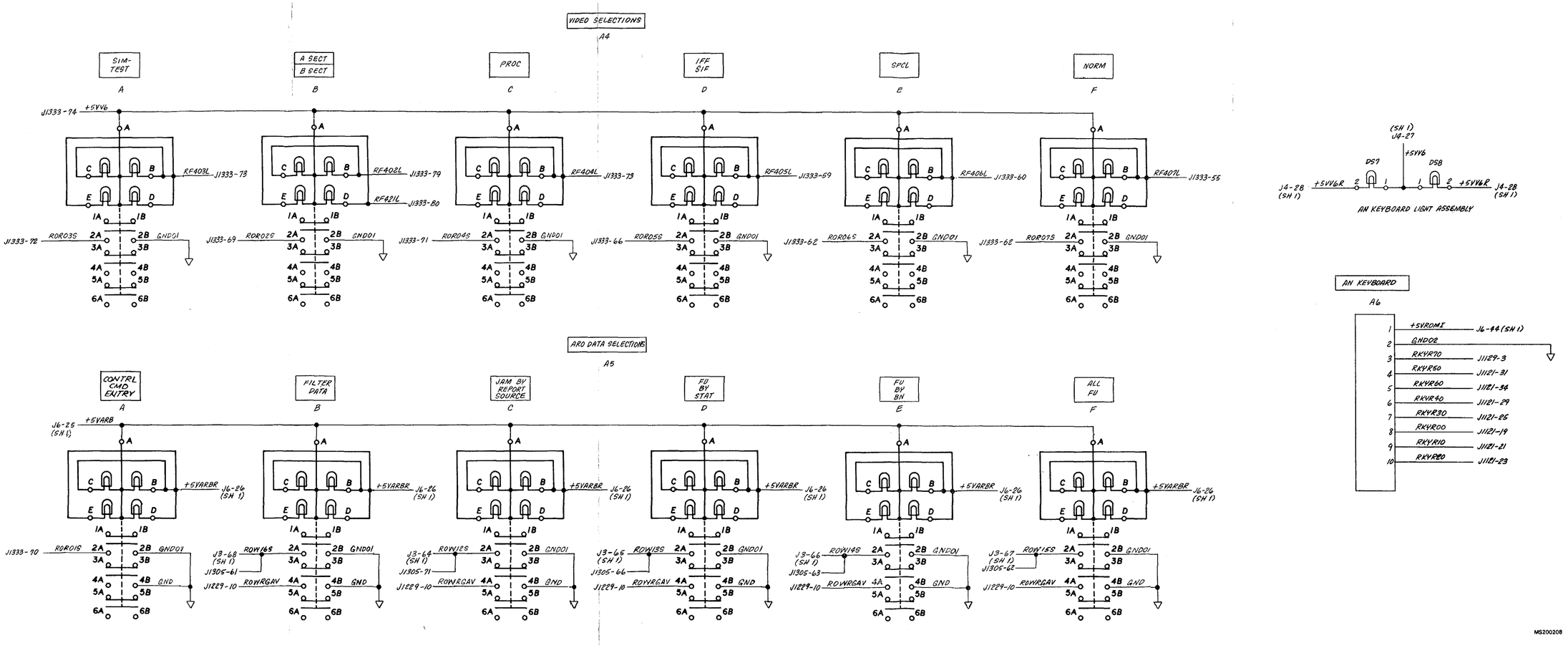
1. ▭ INDICATES FRONT PANEL MARKING.
2. 

INDICATES TYPICAL MECHANICAL CONFIGURATION (SEE A1)
3. 

INDICATES TYPICAL MECHANICAL CONFIGURATION (SEE A4 ON SH 2)

MS200207

FO-63. Right Hand Font Panel, Schematic Diagram (Sheet 1 of 2)



MS200208

FO-63. Right Hand Font Panel, Schematic Diagram (Sheet 2 of 2)

By Order of the Secretary of the Army:

JOHN A. WICKHAM, JR.
General, United States Army
Chief of Staff

Official:
DONALD J. DELANDRO
Brigadier General, United States Army
The Adjutant General

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THE METRIC SYSTEM AND EQUIVALENTS

'NEAR MEASURE

. Centimeter = 10 Millimeters = 0.01 Meters = 0.3937 Inches
1 Meter = 100 Centimeters = 1000 Millimeters = 39.37 Inches
1 Kilometer = 1000 Meters = 0.621 Miles

'VEIGHTS

Gram = 0.001 Kilograms = 1000 Milligrams = 0.035 Ounces
1 Kilogram = 1000 Grams = 2.2 lb.
1 Metric Ton = 1000 Kilograms = 1 Megagram = 1.1 Short Tons

LIQUID MEASURE

1 Milliliter = 0.001 Liters = 0.0338 Fluid Ounces
1 Liter = 1000 Milliliters = 33.82 Fluid Ounces

SQUARE MEASURE

1 Sq. Centimeter = 100 Sq. Millimeters = 0.155 Sq. Inches
1 Sq. Meter = 10,000 Sq. Centimeters = 10.76 Sq. Feet
1 Sq. Kilometer = 1,000,000 Sq. Meters = 0.386 Sq. Miles

CUBIC MEASURE

1 Cu. Centimeter = 1000 Cu. Millimeters = 0.06 Cu. Inches
1 Cu. Meter = 1,000,000 Cu. Centimeters = 35.31 Cu. Feet

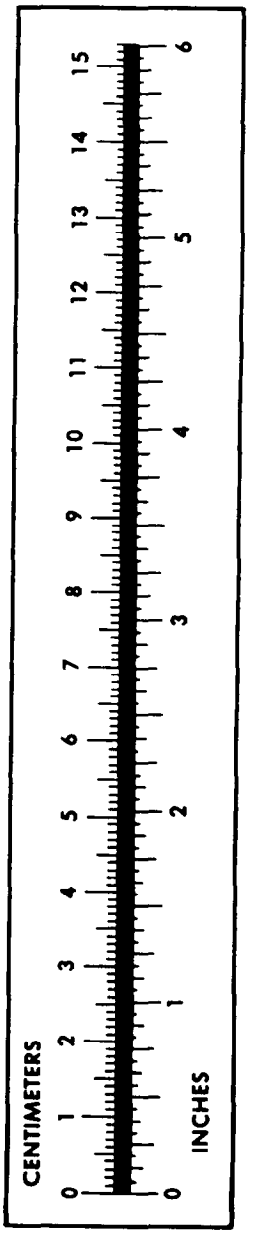
TEMPERATURE

5/9(°F - 32) = °C
212° Fahrenheit is evuivalent to 100° Celsius
90° Fahrenheit is equivalent to 32.2° Celsius
32° Fahrenheit is equivalent to 0° Celsius
9/5C° + 32 =°F

APPROXIMATE CONVERSION FACTORS

TO CHANGE	TO	MULTIPLY BY
Inches	Centimeters	2.540
Feet	Meters	0.305
Yards	Meters	0.914
Miles	Kilometers	1.609
Square Inches	Square Centimeters	6.451
Square Feet	Square Meters	0.093
Square Yards	Square Meters	0.836
Square Miles	Square Kilometers	2.590
Acres	Square Hectometers	0.405
Cubic Feet	Cubic Meters	0.028
Cubic Yards	Cubic Meters	0.765
Fluid Ounces	Milliliters	29.573
ıts	Liters	0.473
arts	Liters	0.946
allons	Liters	3.785
Ounces	Grams	28.349
Pounds	Kilograms	0.454
Short Tons	Metric Tons	0.907
Pound-Feet	Newton-Meters	1.356
Pounds per Square Inch	Kilopascals	6.895
Miles per Gallon	Kilometers per Liter	0.425
Miles per Hour	Kilometers per Hour	1.609

TO CHANGE	TO	MULTIPLY BY
Centimeters	Inches	0.394
Meters	Feet	3.280
Meters	Yards	1.094
Kilometers	Miles	0.621
Square Centimeters	Square Inches	0.155
Square Meters	Square Feet	10.764
Square Meters	Square Yards	1.196
Square Kilometers	Square Miles	0.386
Square Hectometers	Acres	2.471
Cubic Meters	Cubic Feet	35.315
Cubic Meters	Cubic Yards	1.308
Milliliters	Fluid Ounces	0.034
Liters	Pints	2.113
Liters	Quarts	1.057
ers	Gallons	0.264
ms	Ounces	0.035
ograms	Pounds	2.205
Metric Tons	Short Tons	1.102
Newton-Meters	Pounds-Feet	0.738
Kilopascals	Pounds per Square Inch	0.145
lometers per Liter	Miles per Gallon	2.354
meters per Hour	Miles per Hour	0.621



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